DESIGN OF A DIGITALLY

CONTROLLED RING

OSCILLATOR FOR ADPLL

MSc Thesis

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Omar Hamzeh

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By Omar Hamzeh

13 August 2021

We certify that we have read this dissertation and that in our opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Master of Science.

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I hereby declare that all information in this document has been obtained and presented in accordance with the academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

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LIST OF SYMBOLS

L   : Inductor
C   : Capacitor
M   : Mega
Hz   : Hertz
μ   : Micron
$\mathbf{f_0}$: Center Frequency
f   : Frequency
$\mathbf{K_{vco}}$: Voltage Controlled Oscillator Gain
$\mathbf{V_{ctl}}$: Control Voltage
$\mathbf{W_c}$: Capacitor Energy
$\mathbf{W_L}$: Inductor Energy
V   : Voltage
$\mathbf{Z_L}$: Inductor Impedance
$\mathbf{Z_C}$: Capacitor Impedance
ω   : Angular Frequency
R   : Resistor
Ω   : Ohms
$\mathbf{V_{DD}}$: Supply Voltage
$\mathbf{V_{SS}}$: Ground
$\mathbf{t_d}$: Propagation Delay
$\mathbf{C_L}$: Load Capacitor
$\mathbf{R_L}$: Load Resistor
η   : A proportionality constant that is approximately equals 1
K   : Boltzmann's Constant
$\mathbf{V_{char}}$: Overdrive voltage of the device gate
T   : Temperature in K
K   : Kelvin
P   : Total power dissipation
Q   : Quality Factor
$\mathbf{T_{mux}}$: Propagation Delay of Multiplexer
$\mathbf{I_{out}}$: Output Current
n   : Nano
k   : Kilo
G   : Giga
fF   : femtofarad
pF   : Picofarad
Δf   : Frequency Difference

ABBREVIATIONS

IC	: Integrated Circuit
CMOS	: Complementary-Metal-Oxide-Semiconductor
RF	: Radio Frequency
PLL	: Phase-Locked Loop
SoC	: System on Chip
VCO	: Voltage Controlled Oscillator
DCO	: Digitally Controlled Oscillator
AI	: Artificial Intelligence
PD	: Phase Detector
FD	: Feedback Divider
LPF	: Low Pass Filter
SNR	: Signal-to-Noise Ratio
RO	: Ring Oscillator
DAC	: Digital to Analog Converter
DCR	: Digitally Controlled Resistor
MSB	: Most Significant Bits
LSB	: Least Significant Bits
PVT	: Process, Voltage and Temperature changes
WS	: Worst Speed
TM	: Typical Environment
WP	: Worst Power
ANN	: Artificial Neural Network
MSE	: Mean Squared Error
LF	: Learning Factor
RMSE	: Root Mean Squared Error

ADPLL İÇIN SAYISAL KONTROLLÜ HALKA OSİLATÖR TASARIMI

ÖZET

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Sayısal olarak kontrol edilen osilatör, özellikle PLL'lerde geniş kullanımları nedeniyle yaygın olarak araştırılan bir devredir. Bu tez, yeterince geniş bir ayar aralığına ve ince frekans adımlarına sahip, sayısal olarak kontrol edilen bir halka osilatörü önermektedir. Tasarlanan sayısal olarak kontrol edilen halka osilatörü, ADPLL'ye tahsis edildiğinden ve geniş bir ayar aralığı, güç verimliliği ve küçük alan garanti ettiğinden, tek uçlu halka osilatör topolojisine dayanmaktadır. Ana çalışma frekansı gereksinimi, 400 MHz merkezli düşük frekans ve 560 MHz merkezli yüksek frekans olarak verilmiştir. İnce frekans adımları ile yeterince geniş bir ayar aralığı elde etmek ve Proses, Gerilim ve Sıcaklık köşelerini kapsayacak şekilde tasarım, kaba ayar, ince ayar ve işlem köşe ayarı için üç ana ayar ağına dayanır. Bu tasarım, 400MHz'de 1,9MHz ve 560MHz'de 3,8MHz frekans adımı ile (278,9MHz – 1,14GHz) frekans aralığında salınım yapma potansiyeline sahiptir. Ayrıca, ince frekans adımı 37 kHz'dir ve ana besleme voltajı 1,8V'dir. Kapsanan PVT köşeleri %10 voltaj değişimi, sıcaklık aralığı (71º, - 40º) ve teknoloji hızındaki değişim yavaş, tipik ve hızlıdır. 1MHz ofsetinde faz gürültüsü -113,9dBc ve -111,8dBc'dir ve güç tüketimi 400MHz ve 560MHz için sırasıyla 2,86mW ve 3,83mW'dir. Ayrıca bu çalışma, X-Fab tarafından XH018 0,18μm CMOS teknolojisi kullanılarak gerçekleştirilmiştir. Önerilen DCO'nun serimini oluşturmak için beş metal katmanın kullanıldığı Cadence Virtuoso Düzen düzenleyici aracı kullanılarak yapılmıştır. Bu işin üst seviye yerleşim boyutları 245μm genişlik ve 315μm yüksekliktir. Son olarak, bu çalışma, teori ile gerçek tasarım ortamı arasındaki boşluğu kapatmak ve gerekli tasarım süresini azaltmak için yapay sinir ağı algoritmalarına dayalı benzersiz bir tasarım modeli önermektedir. Tasarlanan DCO'yu modellemek için yapay sinir ağı tabanlı bir model tasarlanmıştır. Modeli eğitmek ve test etmek için kullanılan veri seti, tasarlanan DCO sonucundan çıkarılır. ANN modelinin performansı, verilen direnç ve kapasitans için DCO'nun salınım frekansını etkin bir şekilde tahmin eden, MSE'nin 3,95x10-5 ve Kök Ortalama Karesi Hatasının (RMSE) 0,0063 olduğu 2,5 MHz'lik bir ortalama hatayla umut verici sonuçlar verir.

Anahtar sözcükler: ADPLL, PLL, VCO, DCO. Halka Osilatörü.

DESIGN OF A DIGITALLY CONTROLLED RING OSCILLATOR FOR ADPLL

ABSTRACT

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MSc in Electrical, Electronics Engineering and Cyber Systems

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The digitally controlled oscillator is a commonly investigated circuitry due to its wide uses, especially in PLLs. This thesis proposes a digitally controlled ring oscillator with a sufficiently wide tuning range and fine frequency steps. The designed digitally controlled ring oscillator is based on single-ended ring oscillator topology since it is dedicated to ADPLL and guarantees a wide tuning range, power efficiency and small area. The main operation frequency requirement is given as low frequency centered at 400MHz and high frequency centered at 560MHz. In order to obtain a sufficiently wide tuning range with fine frequency steps and to cover the Process, Voltage, and Temperature corners, the design relies on three main tuning networks for coarse tuning, fine-tuning and process corner tuning. This design has the potential of oscillating at the frequency range of (278.9MHz - 1.14GHz) with a frequency step of 1.9MHz at 400MHz and 3.8MHz at 560MHz. Moreover, the fine frequency step is 37 kHz and the main supply voltage is 1.8V. The PVT corners covered are 10% voltage change, the temperature range of (71º, - 40º), and the change in the technology speed as slow, typical, and fast. The phase noise is -113.9dBc and -111.8dBc at 1MHz offset and the power consumption is 2.86mW and 3.83mW for 400MHz and 560MHz respectively. This work was implemented using XH018 0.18μm CMOS technology by X-Fab. The layout design was done using Cadence Virtuoso Layout editor tool, where five metals layers were used to construct the layout of the proposed DCO. The Top-level layout dimensions of this work are 245μm in width and 315μm in height. Finally, this work proposes a unique design model based on artificial neural network algorithms in order to cover the gap between theory and the real design environment and to reduce the required design time. An artificial neural network-based model is designed to model the designed DCO. The dataset used for training and testing the model is extracted from the designed DCO outcome. The performance of the ANN model gives promising results predicting the oscillation frequency of the DCO effectively for the given resistance and capacitance with an average error of 2.5MHz, where MSE is 3.95x10-5 and Root Mean Squared Error (RMSE) is 0.0063.

Keywords: ADPLL, PLL, VCO, DCO. Ring Oscillator.

CHAPTER 1

1. INTRODUCTION

1.1. Motivation and Purpose

Nowadays, Integrated Circuit (IC) technology becomes part and parcel of any system or device that includes Radio Frequency (RF), Communication, Analog, and Digital applications. The evolution of integrated circuit technology has resulted in new challenges and opportunities. In the recent decade, the goal has been to design smaller portable solutions with low power consumption and small chip areas.

Phase-Locked Loops (PLLs) are fundamental components of every System on Chip (SoC) or device due to the precious functionality they provide. PLLs are used as clocks for digital system, frequency synthesizers for communications applications, and RF carrier signals generators for wireless communication systems. The Voltage-Controlled Oscillator (VCO) is the most critical component of the PLL since it generates and delivers the output signal of the PLL ranging from low-frequencies to high-frequencies and thus, it is extensively researched [1]-[9]. The VCO architectures are classified into two main types: Ring Oscillators (RO) and LC oscillators. While LC oscillators perform better in terms of phase noise than ring oscillators, ring oscillators still have a major advantage. They typically occupy a tiny area and can be easily integrated with digital CMOS circuitry, hence less cost. Moreover, they have a better tuning range than LC oscillators, which makes them more immune to process, voltage, and temperature (PVT) variations [10],[11]. In spite of the extensive use of the ring oscillator, the modeling and the analysis processes are still serious challenges. The design of a VCO comprises many challenges and tradeoffs. These challenges include oscillation frequency, tuning range, power consumption, area, noise performance, and output waveform.

The aim of the work in this thesis is to design a Digitally Controlled Oscillator (DCO) that is dedicated to be used in an ADPLL with the emphasis to cover the two main center frequencies of 400MHz and 560MHz. The target requirements considered for this work consist of low power consumption, wide tuning range, efficient phase noise performance, and small chip size. Moreover, this work presents a unique modeling approach based on Artificial Intelligence (AI) algorithms in order to narrow down the gap between theory and real design environments and reduce the required design time.

1.2. Tools and Technology

During the design process for the work presented in this thesis, the schematic design, layout design and simulations are implemented using Cadence Virtuoso Design Suite. The work is based on 0.18μm CMOS technology of XH018 by X-Fab. MATLAB platform is used in the process of Artificial Intelligence (AI) modeling part in the attempt to model the DCO.

1.3. Thesis Organization.

Chapter 2 focuses on the literature view of phase locked loops and voltage-controlled oscillators. Furthermore, it studies the working principle and the performance metrics of the voltage-controlled oscillator.

Chapter 3 defines and discusses experimental part of the proposed design architecture and the tuning schemes.

Chapter 4 discusses the performance of the proposed design and presents the results.

Chapter 5 presents the artificial intelligence model that predicts the frequency value for the corresponding DCO parameters with respect to the environment and technology of this work.

Chapter 6 summarizes the overall design proposed in this thesis and concludes the thesis with future work.

CHAPTER 2

2. THEORETICAL PART

This chapter is focused on the literature view of Phase Locked Loop and in deeper details about Voltage Controlled Oscillator (VCO), since the work presented in this thesis is proposing the design of a Digitally Controlled Oscillator (DCO). In the voltage-controlled oscillator section, theory, working principle, performance metrics of the voltage-controlled oscillators are studied.

2.1. Phase Locked Loop (PLL)

In this section, a brief study of the PLL concept is presented, starting with an introduction followed by the types of the PLL.

2.1.1. Introduction

Nowadays, it is rare for any device to be kept devoid of Phase-Locked Loops (PLL) since they are one of the critical blocks used for RF carrier and clock generation in communication applications, RF/ analog, and digital circuits. A Phase-Locked Loop is analyzed as a feedback system in general as depicted in **Figure 2.1** where this feedback system is mainly a combination of a Voltage-Controlled Oscillator (VCO), Phase Detector (PD), Feedback Divider (FD) and a Low Pass Filter (LPF). This combination may vary based on the type of the PLL if it is an analog or digital PLL. PLL is essentially used for radio frequency generation, frequency synthesis, digital clock generation, and data recovery. The first essential element is the Phase Detector (PD) where a portion of the VCO signal is fed back to PD after it is divided by the Feedback Divider (FD) to match the reference frequency. The PD compares the signal coming from FD with the reference signal producing a phase error signal which is proportional to the relative phase of VCO signal and the reference signal. The error signal is then
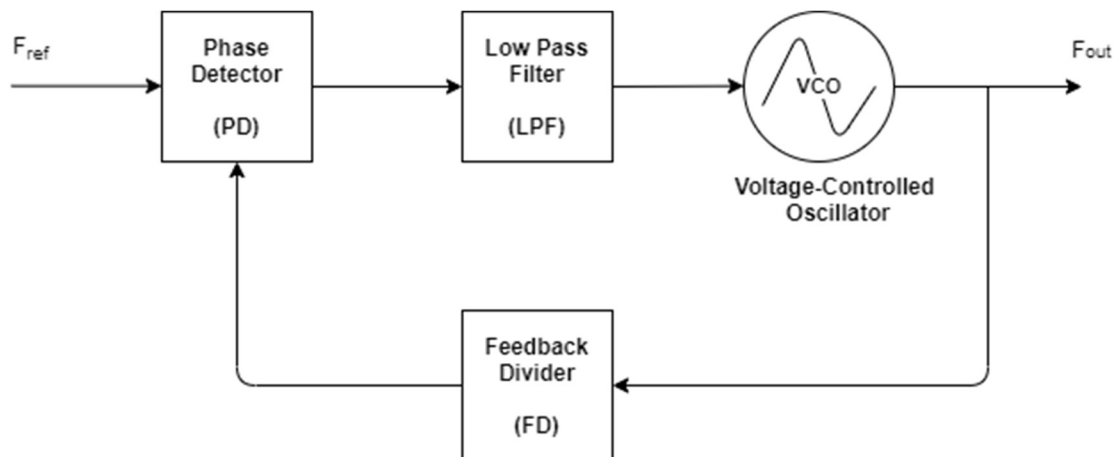
Figure 2.1: Basic PLL diagram.

passed through an LPF removing the high frequency content only the low frequencies are passed. The output of the LPF is a proper control voltage that is fed to the VCO. In response to this control signal, VCO frequency either increases or decreases accordingly until the average of the error signal out of the PD is constant meaning that the reference signal and VCO signal are same in frequency, thus the loop is locked [12],[13].

Phase Locked Loop Types;

- Analog or Linear PLL: All blocks inside the PLL structure are analog blocks.
- Digital PLL: The Phase Detector (PD) is a digital block and the rest of the blocks are analog.
- All digital PLL: All the building blocks used inside the PLL structure are digital blocks.
- Software PLL: The PLL functionality is performed by a software controlling an hardware [12].

2.2. Voltage Controlled Oscillators (VCO)

The main focus of the literature review given in this section is an introduction on the VCO and more specific details are discussed including; theory of oscillation, performance metrics, VCO architectures with comparison and tuning methods.

2.2.1. Introduction

The Voltage-Controlled Oscillator (VCO) is considered as the heart of the PLL because of the functionality and tunability feature that allows the VCO to generate and control the PLL oscillation frequency according to the below equation;

$$f_{VCO} = f_o + K_{VCO}\, V_{ctl} \qquad\qquad (2.1)$$

f_0: Free running VCO frequency where it oscillates without control.

K_{vco}: VCO gain which represents the VCO frequency resolution meaning that the change in VCO frequency caused by the change in control signal.

V_{ctl}: VCO control signal.

The desired behavior of the VCO is to control the output frequency from one frequency to another covering the required frequency tuning range as shown in **Figure 2.2.**
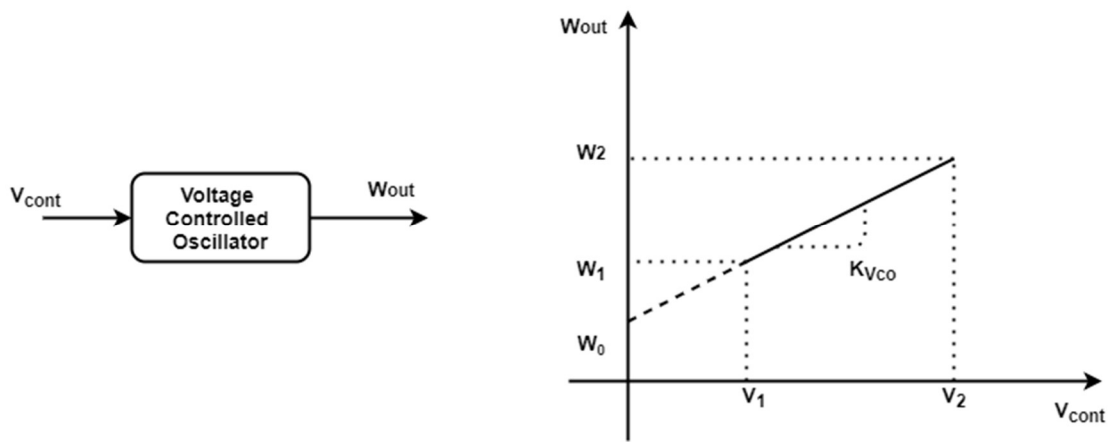
Figure 2.2: Definition of gain KVCO. (Frequency changes due to voltage changes).

The main VCO architectures are the Ring Oscillator (RO) and LC oscillators. These two architecture categories are built on analog based control or digital-based control which is called a Digitally controlled oscillator. This chapter will discuss the main working principle of the VCO, the significance as well as the differences of each VCO architectures and the major parameters that define the VCO performance such as phase noise and the tunable frequency range [14].

2.2.2. Barkhausen criteria

An Oscillator can be studied as a positive feedback system in which it generates periodic output signals once it simultaneously satisfies Barkhausen Criteria. Barkhausen Criteria states two fundamental conditions for an oscillator to oscillate which are; a unity loop gain and a zero or 360° total phase shift, as it is stated below [15];

- $|H(j\omega)| \geq 1$
- $\angle H(j\omega) = 180°$

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Consider a simple linear feedback system as shown in **Figure 2.3.**

Figure 2.3: A simple feedback system.

The transfer function of the feedback system is represented as the following;

$$\frac{Y}{X}(s) = \frac{H(s)}{1 - H(s)} \tag{2.2}$$

In the above feedback system, the amplitudes of the input noise are negligible unless it is the noise at the frequencies where the oscillation conditions are satisfied according to Barkhausen criteria. The noise at these frequencies will be elevated and accumulated to start oscillating. The signal will face a 180° phase shift as it passes through H(s) with a unity gain **Figure 2.4a** and another phase shift of 180° as it travels around the loop back to the input **Figure 2.4b.** Hence, leading to a total of 360° phase shift as the signal travels around the loop from input to output and back to the input, in which it oscillates with the steady-state signal [16].
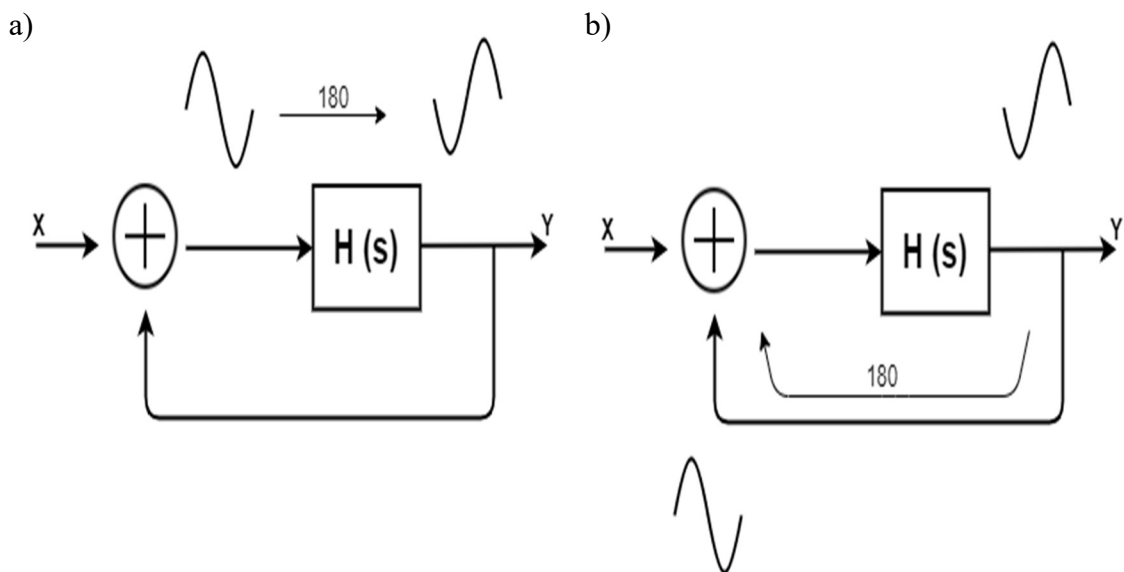
Figure 2.4: Barkhausen's phase shift cycles. a) 180° phase shift due to H(s), b) 360° total phase shift.

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2.2.3. Performance metrics and characteristics of VCO.

2.2.3.1. Frequency tuning range

The tunability feature of the VCO is one of the most significant characteristics where it is needed for most of the applications like the case in wireless applications or radar systems. The VCO tuning range is the range over which the oscillation frequency can be changed from its center frequency. It identifies the maximum and the minimum frequency, and frequency predictability over process and temperature fluctuations. The significance of this feature is that it is required for systems of multiple frequencies. Thus, the tuning range needs to be sufficient to cover the desired possible range of frequencies [14].

2.2.3.2. Frequency resolution

The frequency resolution is a significant characteristic, which determines the scale of the tuning range. The importance of the frequency resolution is also based on the fact that it contributes to the VCO phase noise performance. It is a factor of VCO sensitivity to the changes such as the supply voltage which is called as the VCO gain. It represents the change in VCO frequency caused by the change in control signals as depicted in **Figure 2.2** and given as in equation **(2.1)** [13].

2.2.3.3. Noise

One of the most fundamental VCO characteristics is noise performance of the VCO. Phase noise is considered in frequency domain and jitter is calculated in the time domain. Phase noise significantly effects the desired expected performance of the system degrading the Signal-to-Noise Ratio (SNR). That makes phase noise as the most important parameter for choosing the VCO architecture [17].

2.2.3.4. Power dissipation

When most of the recent applications are considered, power consumed by the oscillator is significant. Low-power design has grown popular in order to keep battery-powered devices functioning for longer periods of time, and also for keeping them light and portable. Moreover, when power usage rises, more heat is dissipated, potentially shortening the device's lifespan. Therefore, power dissipation is a crucial factor to consider when choosing an oscillator topology [17].

2.2.3.5. Manufacturability and area

Advancing in the technology scaling is aiming to integrate as many systems onto a single chip as feasible, so the overall solution can be small while meeting the performance metrics. Furthermore, fitting an entire system into a single chip reduces the overall cost as well as complexity. Therefore, the physical size of the VCO is critical since a larger VCO results in a greater die size, which results in a higher cost [17].

2.2.4. LC Oscillators

2.2.4.1. The work principle of LC oscillator

The LC Oscillators are mainly built using an LC tank where the LC tank consists of a parallel-connected inductor and capacitor. The LC tank structure shown in **Figure 2.5** will simply follow the parallel resonant circuit working principle. The capacitor will store the energy as an electrostatic field where the energy stored in the capacitor is given by;

$$W_c = \frac{1}{2}V^2C \tag{2.3}$$

While the inductor will store energy as an electromagnetic field and the energy stored in the inductor is given by;

$$W_l = \frac{1}{2}I^2L \tag{2.4}$$
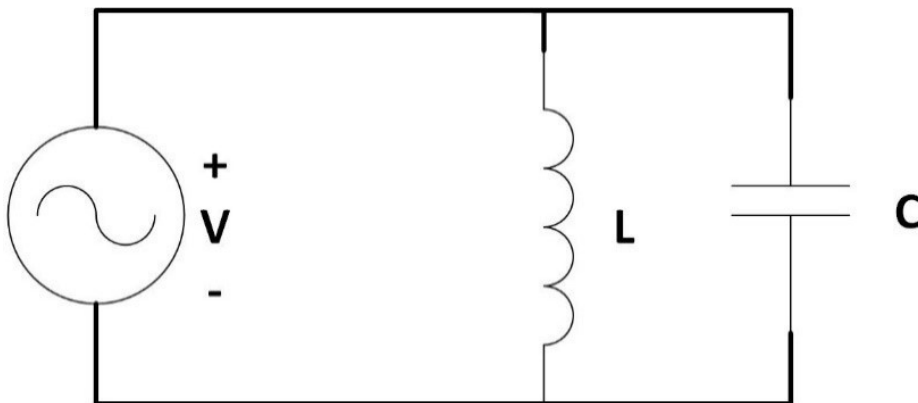
Figure 2.5: Parallel LC Circuit.

This energy transformation will constantly keep going back and forth between the capacitor and the inductor. Hence at a certain frequency, the average energy stored in the capacitor will be equal to the average energy stored in the inductor. Moreover, the impedance of the capacitor will be equal but opposite in phase of the impedance of the

inductor leading that the impedance of the LC-Tank is infinite. As a result of these conditions, the system will produce a continuous oscillation signal at that specific frequency.

The impedance of an inductor is given by;

$$Z_l = j\omega L \tag{2.5}$$

And the impedance of a capacitor is given as below;

$$Z_c = \frac{1}{j\omega C} \tag{2.6}$$

Equating **(2.5)** and **(2.6)** and solving for ω as the resonance frequency gives **(2.7)**;

$$\omega = \frac{1}{\sqrt{LC}} \tag{2.7}$$

However, including the parasitic resistances from the inductor and the capacitor will lead to an energy loss. This is represented in **Figure 2.6.** where R_p is the equivalent resistance causing an energy amplitude decay. Thus, it is required to add an active circuit providing an equivalent negative resistance equals to $| R_p |$ so that the system is able to sustain the oscillation [14], [18].
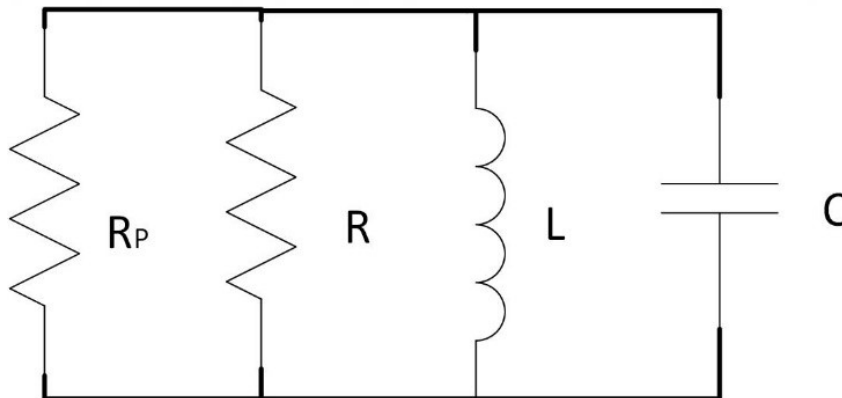
Figure 2.6: LC Oscillator circuit including negative resistance Rp to cancel losses.

2.2.4.2. The cross-coupled LC oscillator

A Cross-Coupled Oscillator is one of the most significant oscillators that is used in practice. The topology that is shown in **Figure 2.7a** represents the simple cross-coupled oscillator. This topology is considered as highly sensitive to the supply voltage as the V_{GS} of the two transistors is equal to V_{DD}. Thus, in order to minimize the supply sensitivity of the oscillator, a tail current source is added, **Figure 2.7b,** to reconstruct the cross-coupled oscillator as a differential pair which is more robust [16].

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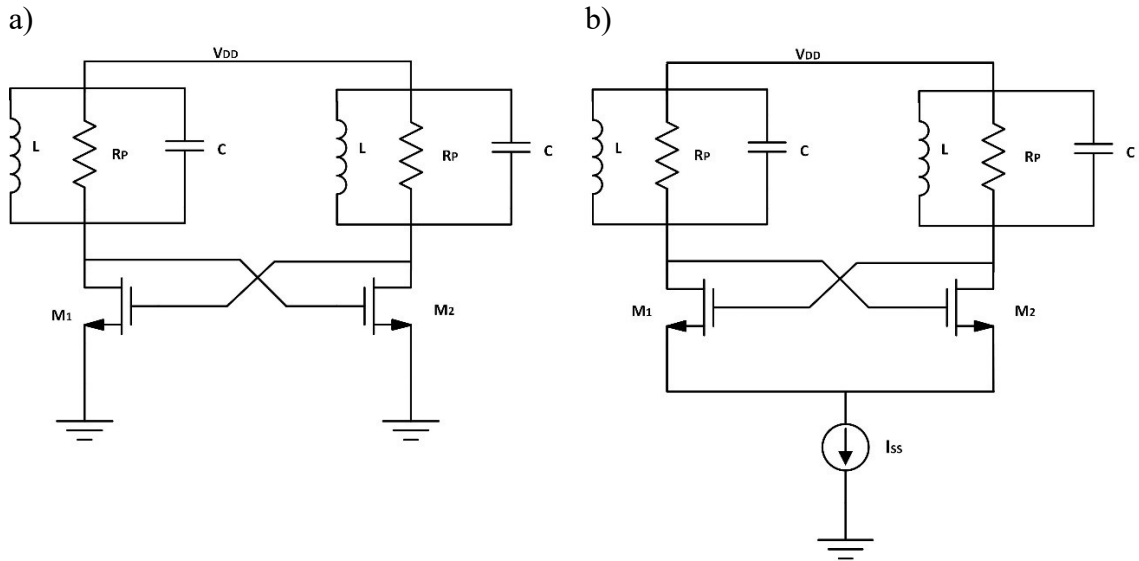
Figure 2.7: a) Simple cross-coupled LC Oscillator. **b)** addition of tail current.

Examining the series combination of the two identical tanks in the cross-coupled oscillator leads to construction of a tank model merging the two tanks into one as depicted in **Figure 2.8.**
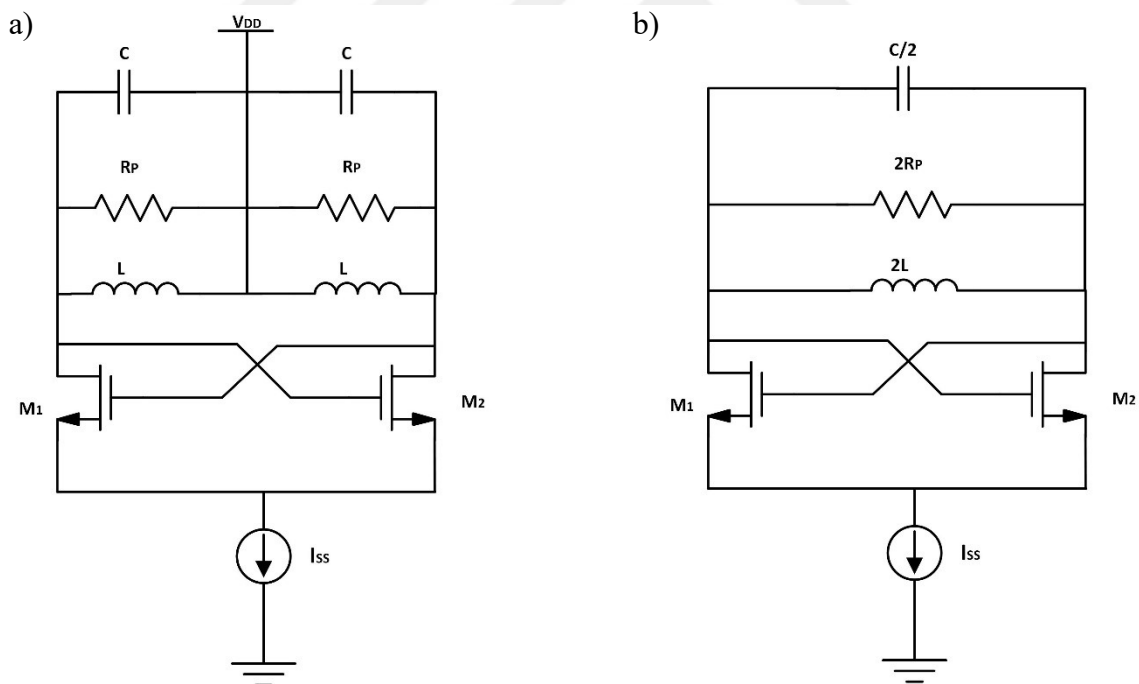
Figure 2.8: a) rebuilding of cross-coupled LC Oscillator. **b)** load tanks merged.

The resulting oscillator can be studied as a lossy resonator having a single tank that consists of C/2, 2L and $2R_p$. The equivalent impedance of the cross-coupled tank is calculated in the equation **(2.8)** below since $g_{m1} = g_{m2} = g_m$

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$$G_x = \frac{i_x}{v_x} = -\frac{g_m}{2} \qquad (2.8)$$

Hence, in order for the oscillation to occur, the negative resistance of the active circuit must be able to cancel the loss of the tank;

$$\frac{2}{g_m} \leq R_p \qquad (2.9)$$

Thus,

$$g_m R_p \geq 1 \qquad (2.10)$$

This condition ensures the oscillation. However, when gm is exactly equal to 1/R_p, the output oscillation signal will be weak leading to a poor phase noise. Therefore, it is worth picking gm value much larger than just 1/R_p [19].

2.2.4.3. The three-point oscillator

According to the LC oscillator work principle discussed before and recalling the basic transistor amplifier structures, three different oscillator topologies can be constructed by ac grounding the drain, the gate, or the source forming Clapp oscillator, Colpitts oscillator or source grounded oscillator. **Figure 2.9.**
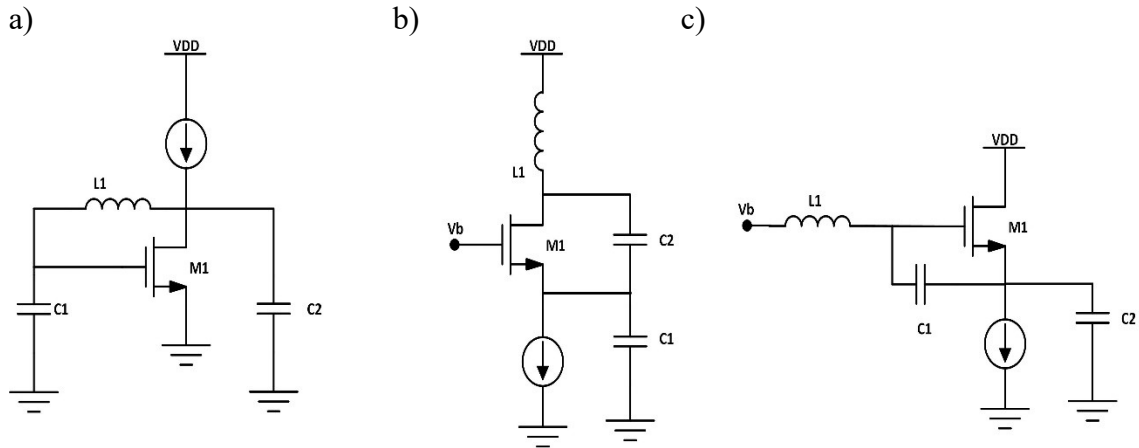
Figure 2.9: Three-Point Oscillators. **a)** with source grounded. **b)** with gate grounded (Colpitts Oscillator). **c)** with drain grounded (Clapp Oscillator).

The resulting oscillator topologies follow the same operation frequency formulas and the tank model of the three topologies will be the same, if the parasitic capacitors are not included;

$$\omega_{osc} = \cfrac{1}{\sqrt{L_1 \cfrac{C_1 C_2}{C_1 + C_2}}} \qquad (2.11)$$

Moreover, these three topologies must have sufficient transconductance in order for the oscillation to occur;

$$g_m R_p = \frac{C_1}{C_2} + \frac{C_2}{C_1} + 2 \qquad (2.12)$$

Thus, the minimum allowable transconductance, when $C_1 = C_2$ is given as;

$$g_m R_p \geq 4 \qquad (2.13)$$

The three-point oscillators, require a high inductor Q in order to ensure the oscillator to oscillate. In addition, these three topologies provide a single-ended outputs only [16].

2.2.5. Ring oscillators

2.2.5.1. The working principle of the ring oscillator

Ring oscillators are basically constructed with a chain of delay stages connected in cascade, where the output of each stage is an input for the next one and the output of the last stage is fed back to the first stage as an input. The ring oscillator is the same as other oscillators types where it obeys the Barkhausen criteria in order for the oscillation to occur. For an N-stages ring oscillator, each stage will provide a $180°/N$ of phase shift and the other $180°$ of phase shift is coming from the feedback loop **Figure 2.10.**
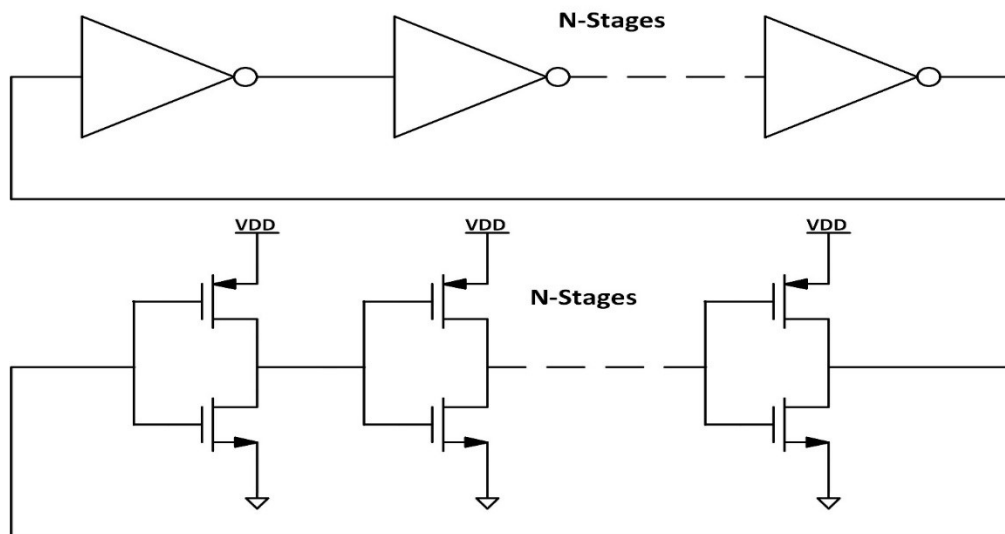
Figure 2.10: Basic Ring Oscillator structure using inverter stages.

The key block in the ring oscillator is the delay stage in which the oscillation frequency mainly depends on the Propagation Delay t_d of the inverter stage as well as the number of stages. Assume that a ring oscillator is built of an N number of stages where each stage gives t_d delay. Thus, the signal requires $N \cdot t_d$ delay passing through all N stages to obtain 180° phase shift. The signal must pass through all the stages the second time in order to obtain the other 180° phase shift, which gives a total of $2 \cdot N \cdot t_d$ time delay for the oscillation to occur. Thus, the oscillation frequency is calculated using the formula **(2.14)** below [20];

$$f = \frac{1}{2 \, N \, t_d} \qquad (2.14)$$

In order to find the t_d propagation delay of a single stage, it is important to study the inverter stage structure. **Figure 2.11** demonstrates a simple delay stage model, where the propagation delay time t_d can be defined as the maximum time required for the input signal crossing 50% to the output crossing 50%.
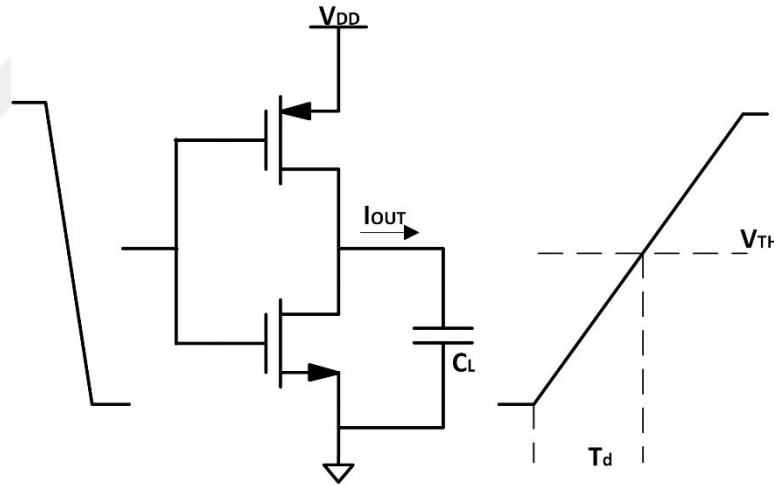
Figure 2.11: Simple delay stage model.

Therefore, t_d is calculated as follows **(2.15)**;

$$\frac{I_{out}}{C_L} = \frac{V_{TH}}{t_d} \; \rightarrow \; t_d = \frac{C_L \, V_{TH}}{I_{out}} \qquad (2.15)$$

This also can be written using the RC delay model as **(2.16)**;

$$t_d = 0.69 \, R C_L \qquad (2.16)$$

Where I_{out} is the output current, C_L is the capacitor load and V_{TH} is the threshold voltage of the device [21].

2.2.5.2. The single-ended ring oscillator

The single-ended ring oscillator is considered the simplest ring oscillator structure and it falls into the same category as discussed in the ring oscillator working principal part. **Figure 2.12** depicts a single-ended ring oscillator constructed with an odd number of delay stages connected in cascade, which provides the gain and phase shift required for the oscillation to occur. The reason behind odd number of stages in the single ended model is to keep the output of each stage switching between 0 and 1 indefinitely.
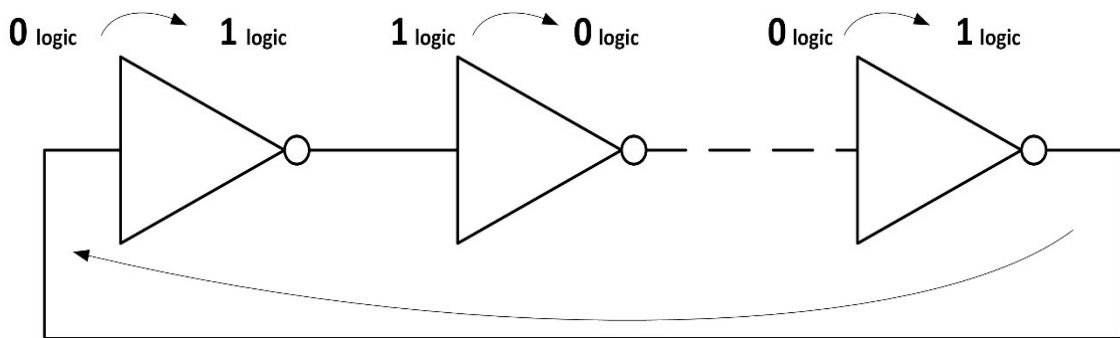
Figure 2.12: Single-Ended Ring Oscillator with single changes.

The structure of the single-ended ring oscillator gives the advantage of the power efficiency where the delay stage draws power only at the transition signal. Moreover, it is capable of providing a full rail-to-rail swinging output signal with a lower jitter as the amplitude is larger.

However, the single-ended ring oscillator suffers from sensitivity to supply and substrate noise. This noise may couple onto the output signal of the single-ended oscillator which will show up as jitter [21].

2.2.5.3. The differential loop ring oscillator

The differential loop ring oscillator consists of differential delay or amplifier stages similar to the case in single ended ring oscillator. It also obeys the Barkhausen criteria for the oscillation to start up, and the signal is defined differentially as depicted in **Figure 2.13.**
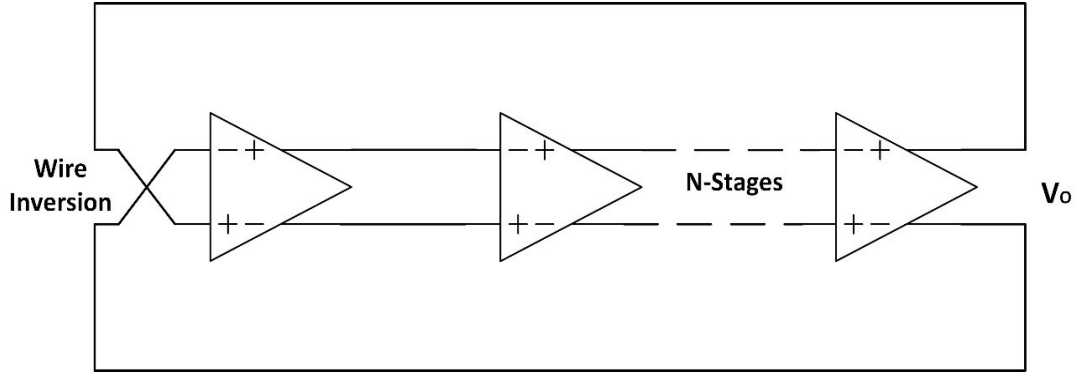
Figure 2.13: Ring Oscillator with differential signal.

The differential loop ring oscillator does not require an odd number of stages since both phases are available and can be used with wire inversion in the differential loop. Moreover, the use of differential circuitry allows for effective common mode rejection. The signal swing of the differential ring oscillator mode is required to be less than the supply voltage in order to keep the devices in the active region so that the common-mode rejection of the differential pair is preserved [21].

2.2.5.4. The pseudo differential ring oscillator

In the pseudo-differential ring oscillator, the signal is defined differentially similar to the differential ring oscillator but pseudo differential delay cells are used for the construction, hence they can provide signal swing of full range from V_{SS} to V_{DD}, improving jitter. However, supply or substrate interference immunity is limited [21].

2.2.5.5. Study on jitter and phase noise

In this study, the expressions used to predict the jitter and the phase noise are focused on single-ended ring oscillator architecture. The ring oscillator is constructed by symmetrical delay devices as much as possible. The resulting equations for phase noise and jitter can be given as **(2.17)** and **(2.18)**;

$$L\{\Delta f\} \approx \frac{8}{3\eta} \frac{kT}{P} \frac{V_{DD}}{V_{cha}} \frac{f_0^2}{\Delta f^2} \qquad (2.17)$$

$$k \approx \frac{8}{3\eta} \frac{kT}{P} \frac{V_{DD}}{V_{char}} \frac{f_0^2}{\Delta f^2} \qquad (2.18)$$

It is worth mentioning that reducing the threshold voltage minimizes phase noise. Thus, the lowest possible phase noise and jitter for a single-ended ring oscillator occurs at zero threshold voltage, if all symmetry terms are satisfied.

$$L\{\Delta f\} > \frac{16\gamma}{3\eta} \frac{kT}{P} \frac{f_0^2}{\Delta f^2} \qquad (2.19)$$

$$k > \sqrt{\frac{16\gamma}{3\eta}} \sqrt{\frac{kT}{P}} \qquad (2.20)$$

Where η is a proportionality constant that is approximately equal to 1,

K is the Boltzmann's Constant,

V_{char} is the overdrive voltage of the device gate,

T is the temperature in K,

R_L is the load resistance,

P is the total power dissipation and,

f_0 is the oscillation frequency.

The minimal phase noise, as can be observed, is inversely related to power dissipation and increases quadratically with oscillation frequency. Yet the single-ended ring oscillator does not require the bias source, hence improves the noise performance excluding the noise corresponding this device [22].

Jitter can be defined in two ways, period jitter and cycle to cycle jitter. Period jitter is defined as the distance between any given clock period and an ideal clock period. It is crucial in synchronous circuits where the lowest possible clock period limits error-free operation and the average clock duration limits circuitry performance. Whereas, cycle to cycle jitter is known as the variation between the durations of two subsequent clock periods where it is very significant concept for clock generation circuits [23].

2.2.6. Ring oscillator versus LC oscillator.

Each of the two main oscillator types that are discussed above have a variety of advantages and suffers from multiple disadvantages. The selection of the oscillator type must be established based on the features and the specifications of the VCO. The main features include; phase noise, maximum frequency, tuning range and manufacturability to choose between an LC or ring oscillator.

2.2.6.1. Phase noise

The most significant specification that needs to meet the project requirement while selecting the oscillator architecture is phase noise. LC oscillator has better phase noise performance compared to ring oscillator in general. Two main factors considered while analyzing the phase noise are the oscillator's achievable quality factor and the oscillator's capacity to reject supply and substrate noise. The quality factor Q of an oscillator is proportional to the circuit's loss, and it is given in **(2.17).**

$$Q = 2\pi \frac{energy\ stoored}{energey\ dissipated\ per\ cycle} \qquad (2.17)$$

The Q of an LC oscillator is higher than that of a ring oscillator. Analyzing the energy storage and dissipation during a cycle reveals the explanation. The energy will pass between the inductive and capacitance elements with no loss in an ideal LC oscillator, resulting in an infinite Q. There are losses associated with each element in a realistic LC oscillator, such as series resistance losses in the inductor, yet energy still shifts between the two reactive parts. In a ring oscillator, however, the energy is stored in the upcoming stage's equivalent capacitance, and the energy is fully charged and subsequently discharged every cycle. The oscillator's ability to reject supply and substrate noise is another reduction source for phase noise. Differential ring oscillators perform better than LC tank oscillators in this regard. The form of supply and substrate noise are two factors that contribute to this advantage. Since the noise sources are closely related, it will affect each stage of the ring oscillator in the same way. As a result, only noise around integer multiples of $N_{\omega 0}$ has an effect on the phase noise. In differential ring oscillators, the control voltage is typically differential, which rejects common mode noise. However, the control voltage in most LC tank oscillators is single ended, making them more vulnerable to noise [14].

2.2.6.2. Maximum frequency

The maximum frequency of the VCO is another specification. In comparison to a ring oscillator, an LC tank has a greater maximum achievable frequency. The square root of L and C determines the LC tank's oscillation frequency. The value of these elements can be set exceedingly low, resulting in a very high tank frequency. Active devices, on the other hand, are still required to keep the oscillation going and can cause to limit the

frequency. Ring oscillators in CMOS have a substantially lower maximum frequency [14].

2.2.6.3. Tuning range

As previously analyzed, a wide tuning range is frequently required to accommodate for process variances or to deal with numerous standards. A ring oscillator should be utilized if a large tuning range is required. There are various parameters that can be changed to modify the frequency of the ring oscillator, as explained in the previous sections, and many of these parameters can be varied across a wide range. Ring oscillators have a tuning range of more than 50%. However, with a monolithic LC tank, the capacitance of the varactor is usually the only variable. This usually results in a tuning range of less than 20% [14].

2.2.6.4. Manufacturability

The VCO's manufacturability is challenged by two factors. These are the efficiency with which the VCO may be integrated into a monolithic application and the amount of variation in the center frequency as a function of process, voltage and temperature parameters. If die area is a major consideration, a ring oscillator is preferable. Monolithic inductors can take up a lot of space, which means they're more expensive. However, due to manufacturing differences, the center frequency of a ring oscillator can fluctuate more than an LC tank. Ring oscillators, despite their larger variance, are more likely to be able to be employed at the appropriate frequency due to their wide tuning range [14].

Table 2.1: The Summary of Ring vs. LC Oscillator.

Summary	Ring Oscillator	LC Oscillator
Phase Noise		X
Maximum Frequency		X
Tuning Range	X	
Manufacturability	X	

2.2.7. VCO tuning methods

The tunability feature of the VCO allows the output frequency to be tuned and controlled as desired. The tuning methods that are studied in this section are mostly focused on Ring Oscillator since the proposed design is based on Ring Oscillator.

Examining a simplified model of ring oscillator as it was studied in section 2.2.5.1, provides the background to understand the tuning methods for the ring oscillator. Tuning methods can be extracted from the equations **(2.14)** and **(2.15).** Tuning frequency can be achieved by changing; [10]

- The number of delay stages N
- The load capacitor C_L
- The voltage V_{TH}
- The drive strength I_{out}.

2.2.7.1. Number of delay stages N

One of the tuning methods is varying the number of delay stages of the ring oscillator using a digital multiplexer to select the number of active stages. **Figure 2.14** is an example of a discrete tuning of ring oscillator using 4:1 multiplexer to change the number of ring stages.
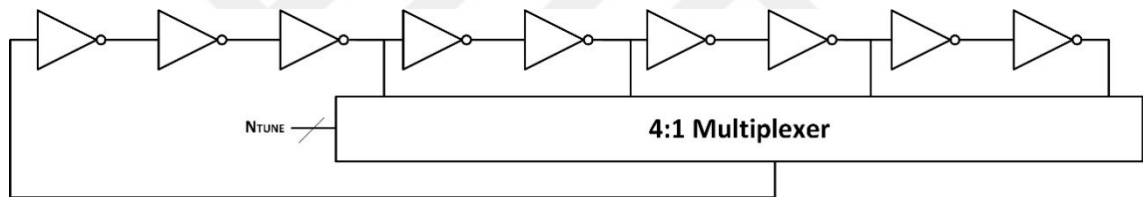
Figure 2.14: Tuning frequency by changing number of delay stages.

Based on the oscillation frequency equation **(2.14)** stated in section 2.2.5.1, the oscillation frequency increases as the number of delay stages decreases. Nine stages ring oscillator is depicted in **Figure 2.14** where the multiplexer controls the stage number via digital code N_{tune} in which 3 stages, 5 stages, 7 stages or nine stages are used to complete the ring oscillator loop.

This method ensures a full digital control as the frequency is controlled using the digital code applied to the multiplexer. Moreover, it provides a wider tuning range due to inclusion of the propagation delay of the multiplexer T_{mux} in to the oscillation equations, thus delay equation becomes;

$$ f = \frac{1}{2\,(N\,t_d + T_{mux})} \tag{2.17} $$

However, varying the number of delay stages to tune the oscillation frequency suffers from large jitter [21].

2.2.7.2. Load capacitor C_L

Tuning the oscillation frequency can be achieved by varying the load capacitance value as well. In this method, the tunability can be based on the type of the capacitance load either varactor or capacitor array. Each delay stage of the ring oscillator will have the same load capacitance in which the control code will be applied on all stages identically. The topology shown in **Figure 2.15a** employs a varactor load in order to tune the oscillation frequency. The varactor or the voltage-controlled capacitor receive the control code V_{ctl} coming from the control DAC that changes the effective varactor capacitance seen at the output of each ring stage. Due to the limited capacitance range that can be varied in most of the varactors, the varactor approach has relatively narrow range of tunability. In order to acquire a wider tuning range, the varactor can be replaced by a set of capacitors as depicted in **Figure 2.15b.** The output capacitance of each delay stage can be controlled using discrete steps of load capacitors as well. The load capacitance will be increased or decreased by activating or deactivating the parallel capacitors respectively, hence the ring oscillator frequency slows down or increases as required [21].

a)   b)

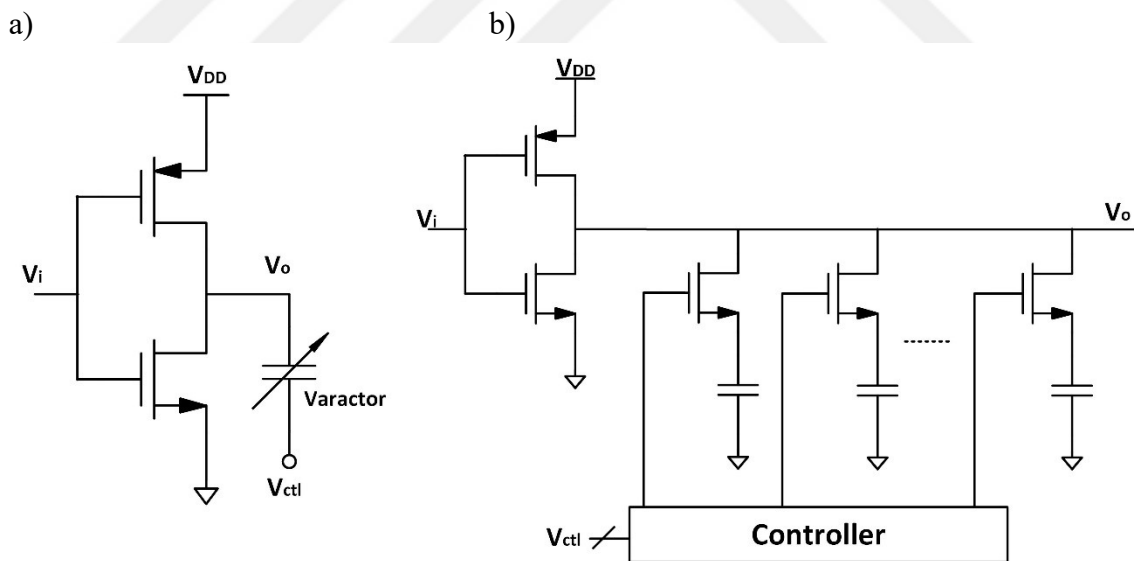**Figure 2.15:** Tuning frequency by varying the load capacitance. **a)** using varactor. **b)** using capacitors.

2.2.7.3. Tuning by voltage V

Another method for tuning the oscillation frequency can be accomplished by adjusting the voltage supply of the ring oscillator or by altering the delay stage threshold. **Figure 2.16** shows a topology that tunes the frequency by varying the supply voltage. The

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supply voltage V_{DD} of the oscillator is varied to a lower or higher voltage which can be implemented by adding a series device from the supply voltage to the ring oscillator or by using a voltage regulator. **Figure 2.16** depicts a Digitally Controlled Resistor (DCR) based ring oscillator where this DCR alters the resistance and change the voltage applied to the ring oscillator, hence changing the oscillation frequency accordingly. This method provides a comparatively wide tuning range compared to the other tuning methods and can reach a very high operating frequency [21].
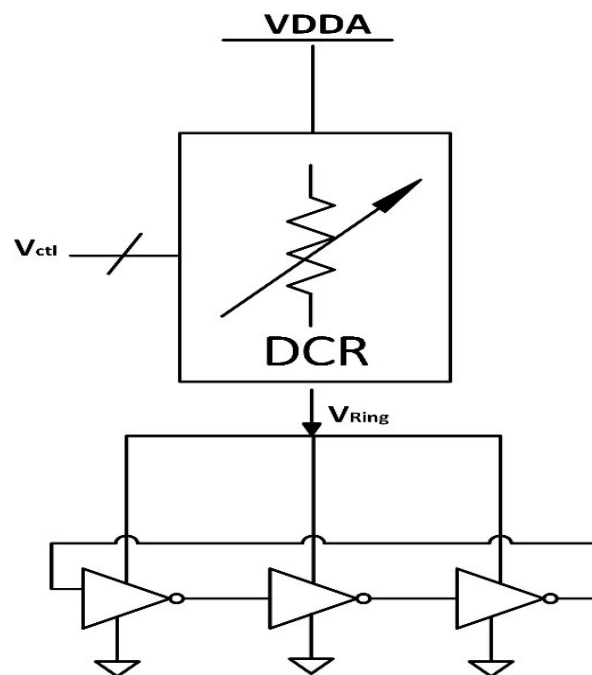
Figure 2.16: A digitally controlled resistors (DCR) based ring oscillator.

2.2.7.4. The drive strength I_{out}

Varying the drive strength of the delay cells is another approach for tuning the oscillation frequency of the ring oscillator. This approach is based on adding devices on series with the ring oscillator in order to change the propagation delay of the ring oscillator stages or to control the current to charge and discharge the load capacitor C_L in order to change the charge up and down times. The circuit in **Figure 2.17** adds an extra PMOS and NMOS transistors in series with the delay stage in order to control the current amount with V_{ctl}. This approach guarantees a wide tuning range, yet the rising and the falling times of the inverter output will not be the same causing a duty cycle problem [21].
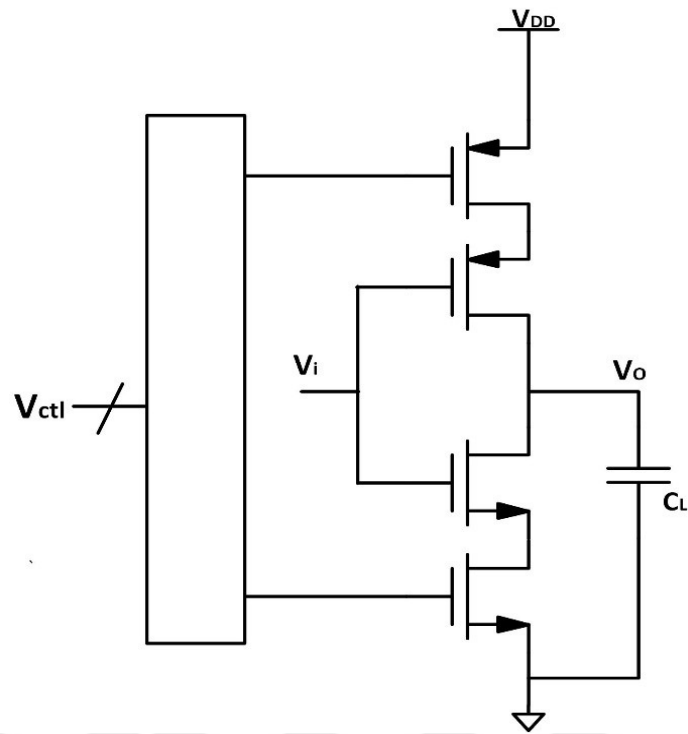
Figure 2.17: A current-starved based ring oscillator.

CHAPTER 3

3.   EXPERIMENTAL PART

In this chapter, a single-ended ring oscillator based digitally controlled oscillator is proposed. The proposed design architecture and the tuning schemes.

3.1.   Topology Selection and Frequency Planning

The proposed digitally controlled oscillator is designed for a PLL used for clocking a system on chip circuit. The fundamental requirements that an oscillator satisfy are the frequency range of operation and drive strength to be able to drive the next stage with an appropriate waveform. The main operation frequency requirement can be given as;

- Low frequency centered at 400MHz
- High frequency centered at 560MHz

The frequency range in this work is selected to be sufficiently wide to ensure it covers the two main centered frequencies. Indeed, this includes an additional range margin for the case of process and temperature variation as well as to cover the modelling inaccuracies. Moreover, the output swing waveform is required to be a square wave since it used as digital clock source. The output voltage swing must be strong enough to drive the necessary building blocks of the PLL. Finally, the design needs to dissipate least amount of power possible and occupy as small area as possible.

3.2.   Digitally Controlled Oscillator Core

The proposed digitally controlled oscillator is based on ring oscillator topology due to the advantages of the ring oscillator that has been discussed in chapter 2. The Tuning methodology of this work relies on three main tuning approaches for coarse tuning, fine tuning and process corner tuning. Each of these approaches is constructed based on one

of the tuning methods studied in chapter 2 in order to meet the tuning range requirements. Since it is a digitally controlled oscillator, all the control circuitry are digital blocks consisting of binary decoders, thermometer decoders and, registers. The DCO block diagram in **Figure 3.1** represents the proposed digitally controlled oscillator.
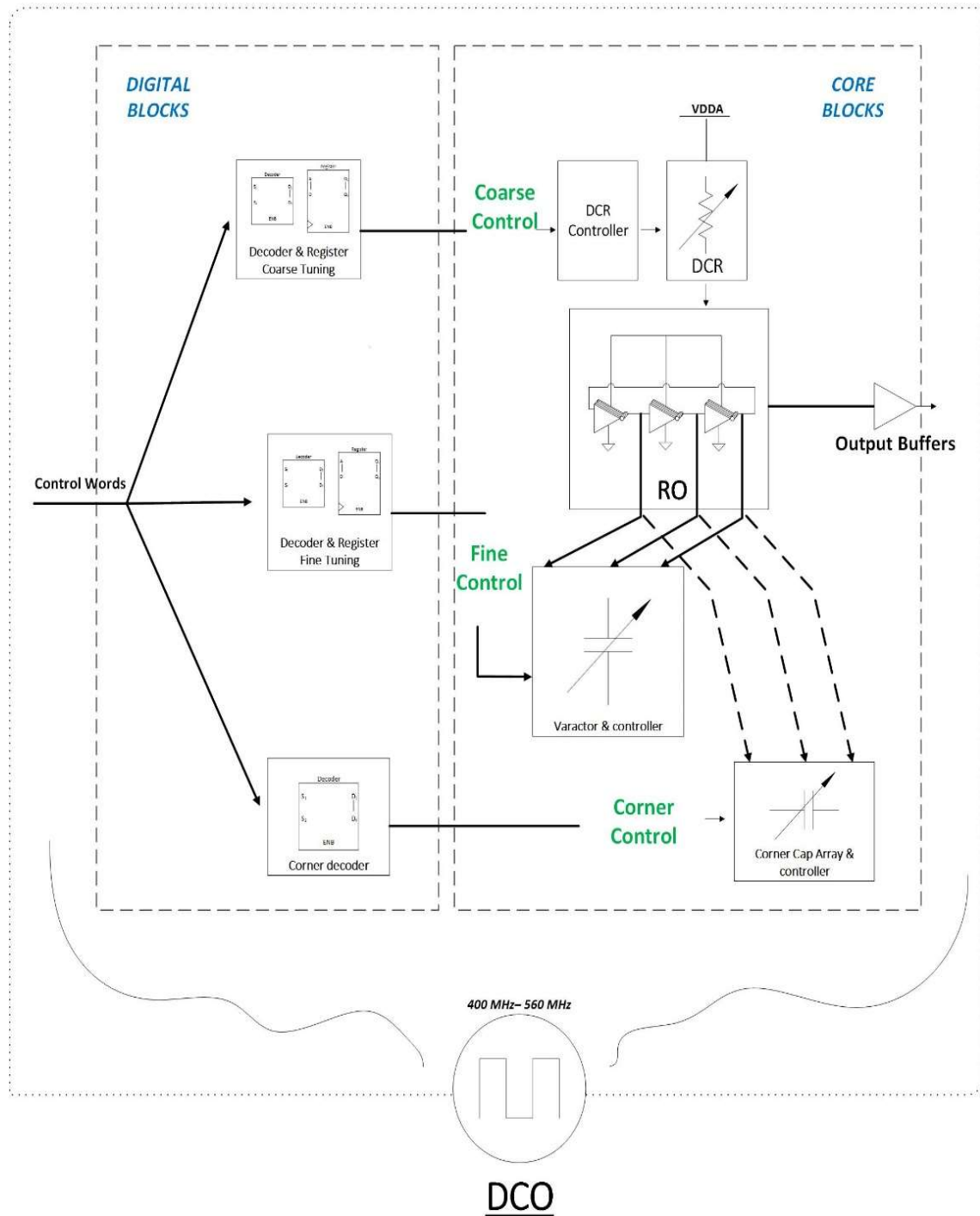
Figure 3.1: The proposed DCO diagram.

3.2.1. Ring oscillator topology

The ring oscillator topology is chosen to be a single-ended one since the structure of the single-ended ring oscillator has the advantage of power efficiency where the delay stage draws power at the transition. Moreover, it is capable of providing a full rail-to-rail output signal with lower jitter as the amplitude is maximized. The design of the delay stage of the ring oscillator is carefully done in order to satisfy the design requirements. The designed ring oscillator depicted in **Figure 3.2** is constructed using three cascaded inverter stages where each stage utilizes five parallel delay units to ensure the strength of the output signal to be able to drive the other blocks as well as to obtain a full rail-to-rail output waveform.
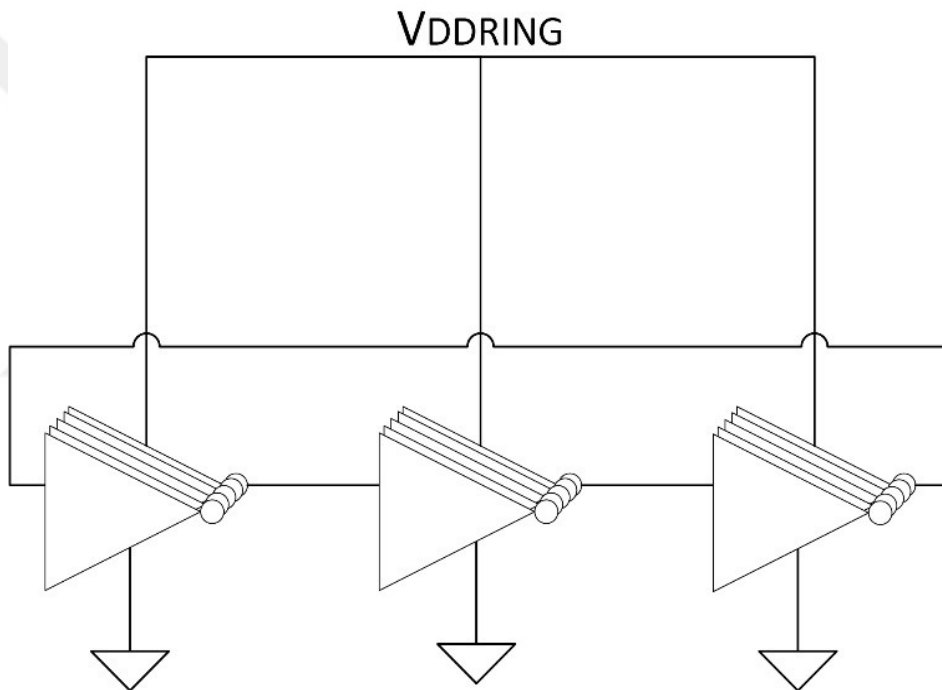
Figure 3.2: The proposed 3 stages Ring Oscillator.

3.2.2. Coarse tuning network

One of the tuning approaches used in this work, is coarse tuning which is based on a digitally controlled resistor (DCR). As it is discussed in chapter two, this method gives a relatively wide tuning range and can reach a very high operating frequency as well. These two advantages make this method favored as it fits the design requirements and cover the needed frequency range effectively. The tuning gain achieved by this method

is high compared to fine tuning methods, which is required in order to cover a wide tuning range. The step resolution or the tuning gain is given in the equation **(3.1)** below;

$$K_{VCO} = \frac{\Delta f}{2^N} \qquad\qquad (\mathbf{3.1})$$

Where K_{vco} is the tuning gain which represents the step resolution meaning the minimum step jump from one frequency to next one,

Δf is the tuning frequency range (high frequency – low frequency),

N is the number of control bits.

Two essential factors are considered for specifying the resolution of the designed DCR; the tuning range and the frequency step. The control code of the DCR is divided into two parts since the structure is composed of rows resistors and columns resistors. The effective role of the row resistors is defining the minimum and maximum frequency corners that the DCR can reach. In other words, the resolution of row resistors determines the lowest and the highest frequency that the RO can oscillate at. On the other hand, the column resistors are responsible for the linearity of the steps which determines the frequency changes from one frequency to another. The DCR shown in **Figure 3.3** demonstrates a DCR of AxB dimensions. The resistor R_{00} as it is called R_{TOP}, has a resistance value of 2R where R is defined as the standard unit resistance value of the DCR. The equivalent resistance of each row resistors excluding the first column resistors is equal to 2R as well. The resistance value of each resistor in the first column excluding R_{TOP}, has value of R. Hence, the equivalent resistance value of the full row equals to R. The first-row resistance value is calculated as in **(3.2)**;

$$R_{1st\text{-}row} = R_{TOP} \text{ // } (R_{01} \text{ // } R_{02} //... \text{ } R_{0B\text{-}2} // R_{0B\text{-}1}) = R \qquad (\mathbf{3.2})$$

The reason behind only R_{TOP} has a value of 2R and the rest at the same column has a value of R only, is that once the first row is activated, the equivalent resistance is R as found in **(3.2)**. Thus, it will be added in series with the next resistor in the first column resulting to have 2R again. Equation **(3.3)** explains the calculation of a full row resistance where x is from 1 to A-1

$$R_{row} = (R_{x0} + R_{(x\text{-}1)0}) // (R_{x1} \text{ // } R_{x2} //... \text{ } R_{xB\text{-}2} // R_{xB\text{-}1}) = R \qquad (\mathbf{3.3})$$

The total resistance loaded when the DCR is fully active equals to R and this represents the minimum resistance load which corresponds to the highest oscillation frequency the

ring oscillator can achieve. In contrast, the ring oscillator will oscillate at the lowest possible oscillation frequency when DCR is inactive meaning that only the first column is on and the rest are off. Equations **(3.4)** and **(3.5)** give the minimum and the maximum achievable resistance of DCR respectively [24];

$$R_{min} = R \tag{3.4}$$

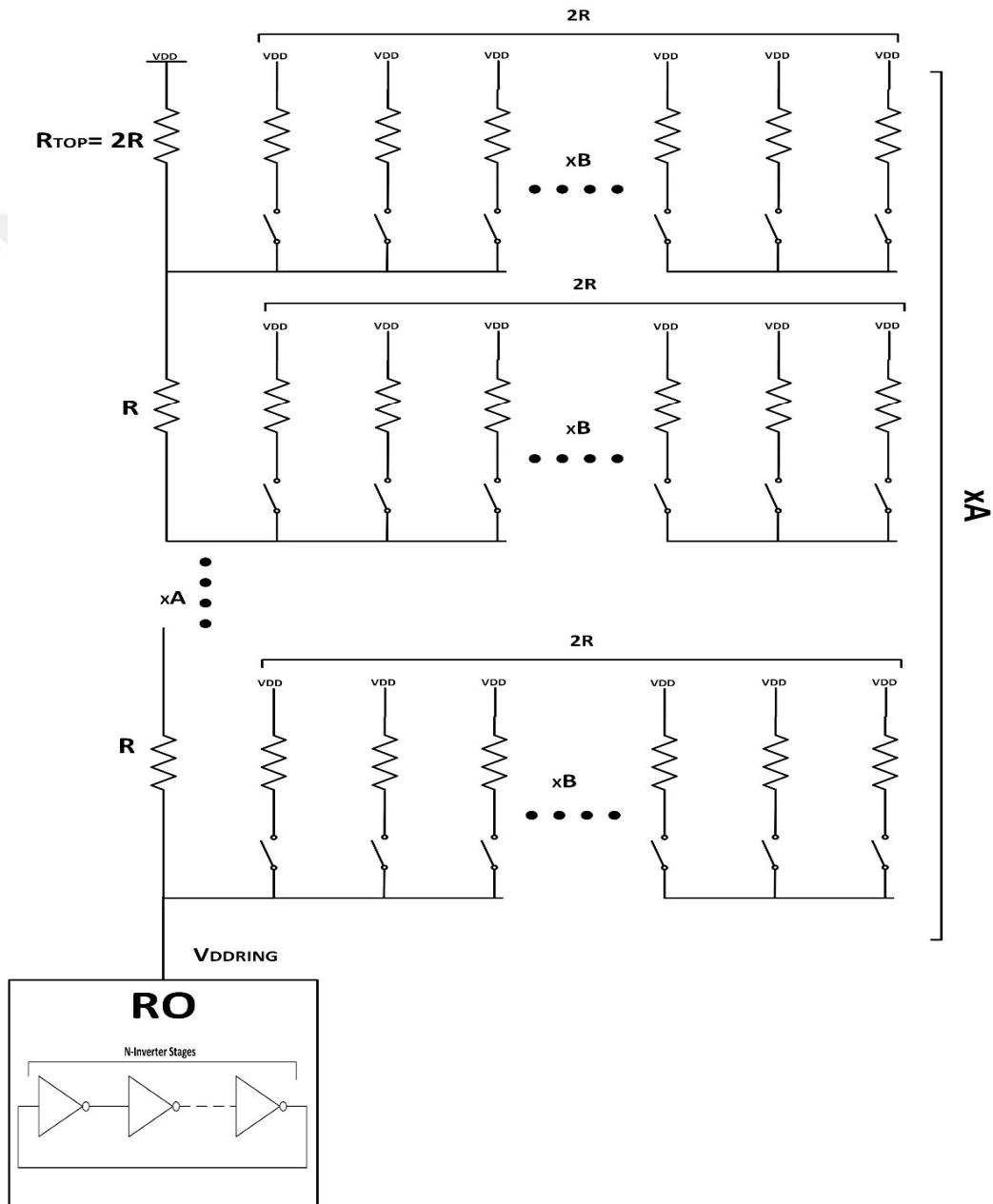$$R_{max} = R_{TOP} + R_{10} + R_{20} + \ ... \ + R_{(A-2)\,0} + R_{(A-1)\,0} = (A+1)R \tag{3.5}$$

Figure 3.3: The Proposed DCR structure.

3.2.3. Fine tuning network

Due to the relatively big tuning steps in the coarse tuning, a second tuning network is introduced in order to achieve fine resolution tuning steps. The fine-tuning network is based on varying the load capacitance of the ring oscillator stages. As it is discussed in chapter two, this method is limited to a narrow range of tunability due to the limited capacitance range that can be varied in most of the varactors. However, it provides sufficiently small steps in order to achieve a fine-tuning resolution. A digitally controlled RC DAC is proposed to control the varactor load of the ring oscillator as depicted in **Figure 3.4**. The same step resolution K_{VCO} formula as shown in equation **(3.1)** applies to this tuning method as well. The proposed digitally controlled RC DAC consists of two parts; a resistor ladder and a switched capacitor array. The resistor ladder works as a voltage divider, which divides the supply voltage into 2^M levels where M represents the number of control bits dedicated to the resistor ladder part. It provides two voltage levels as V_h and V_L for each single control bit. The two voltage levels are calculated as in **(3.6)** and **(3.7)** where X ranges from 1 to 2^M.

$$V_h = \frac{X}{2^M} V_{DD}$$

(3.6)

$$V_L = \frac{X + 1}{2^M} V_{DD}$$

(3.7)

These two voltage levels are applied to the switched capacitors array part where the capacitors are charged and discharged sequentially to a load capacitor providing the required varactor control voltage [25].
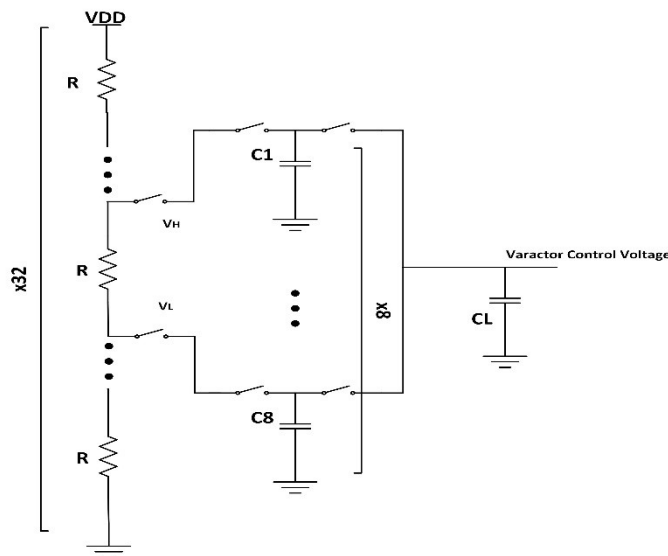

Figure 3.4: The proposed digitally controlled RC DAC.

3.2.4. Process corner tuning network

A third tuning technique is included in this work due to Process, Voltage and Temperature changes (PVT). PVT changes degrade the overall performance and negatively effect the expected outcomes of the design. The PVT corners covered in the present work are 10% voltage change, the temperature range of (71º, -40º) and the change in the process speed as slow, typical and fast process. The main supply voltage used for the proposed DCO is 1.8V, thus 10% voltage change means voltage corners of 1.62V to 1.98V. The correction method relies on varying the load capacitance of the ring oscillator. A switched capacitor array is designed and added to the output capacitance load of the ring oscillator. It consists of a set of parallel capacitors and depending on the PVT corner capacitance added or removed from the output of the ring oscillator in order to fulfill the oscillation frequency requirement precisely. **Figure 3.5** illustrates the structure of the switched capacitor array.
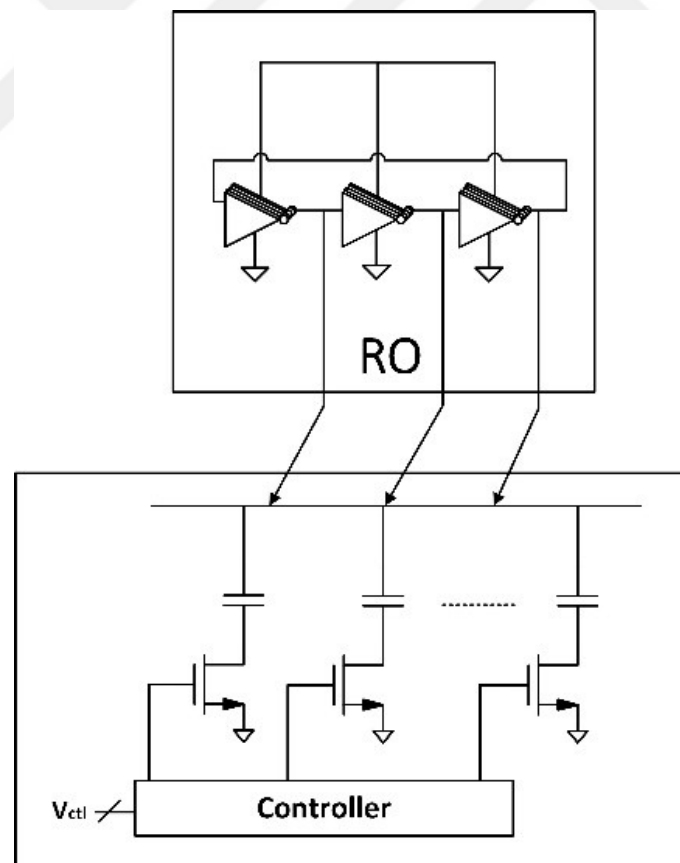
Figure 3.5: The structure of the switched capacitor array.

CHAPTER 4

4.   RESULTS AND DISCUSSION

In this chapter, the proposed digitally controlled ring oscillator architecture and the tuning schemes including the performance metrics and results are discussed below.

4.1.   Ring Oscillator Part

The designed ring oscillator is constructed using three cascaded inverter stages where each stage utilizes five parallel delay units. **Figure 4.1** to **Figure 4.4** show the output waveform of the designed ring oscillator including the rise/fall time. The parameters of the delay stage shown in **Table 4.1** are selected to ensure the Rise/Fall time constant match.

Table 4.1: The parameters of the inverter stage used in ring oscillator.

Inverter Stage	Finger Width (µm)	Finger Count	Multiplier	Total Width (µm)	Length (nm)
PMOS	4	5	1	20	270
NMOS	1.38	5	1	6.9	270

Figure 4.1: Output waveform of the designed ring oscillator.

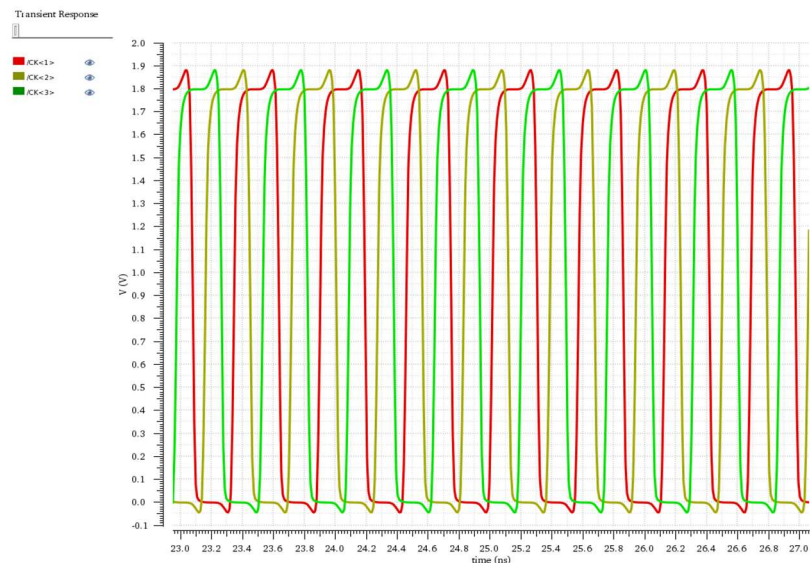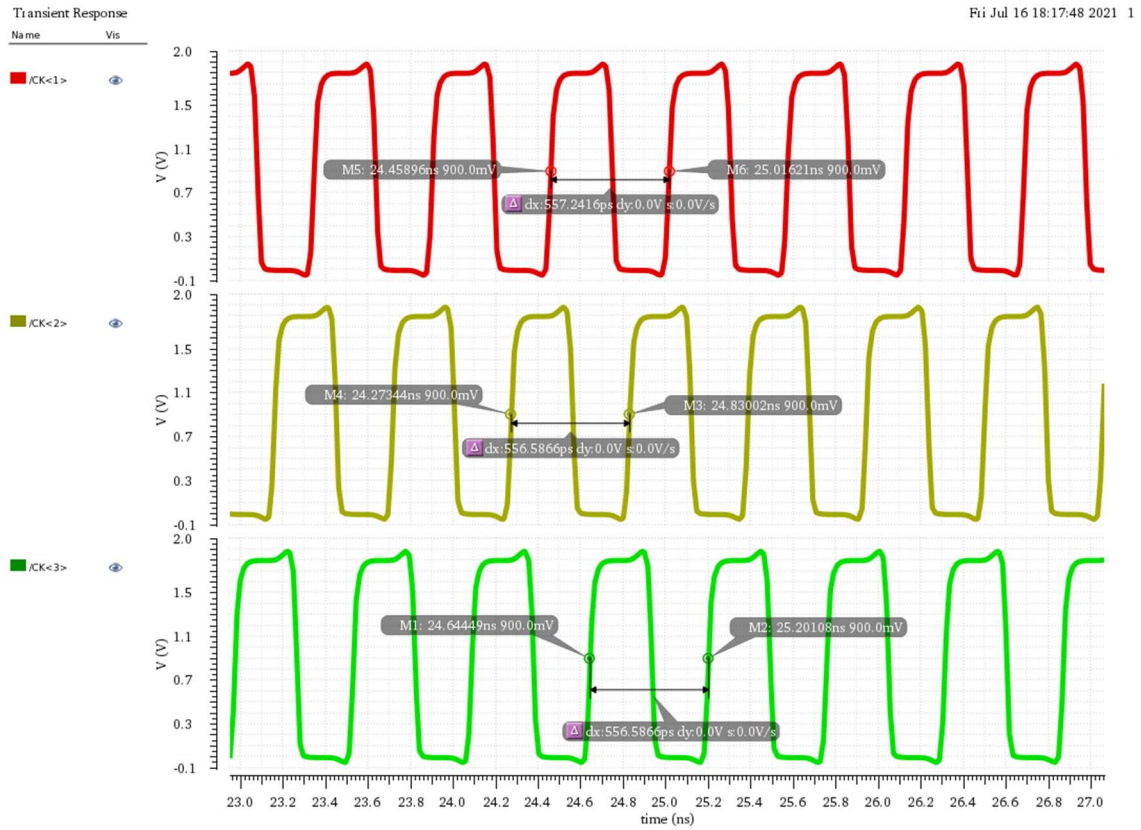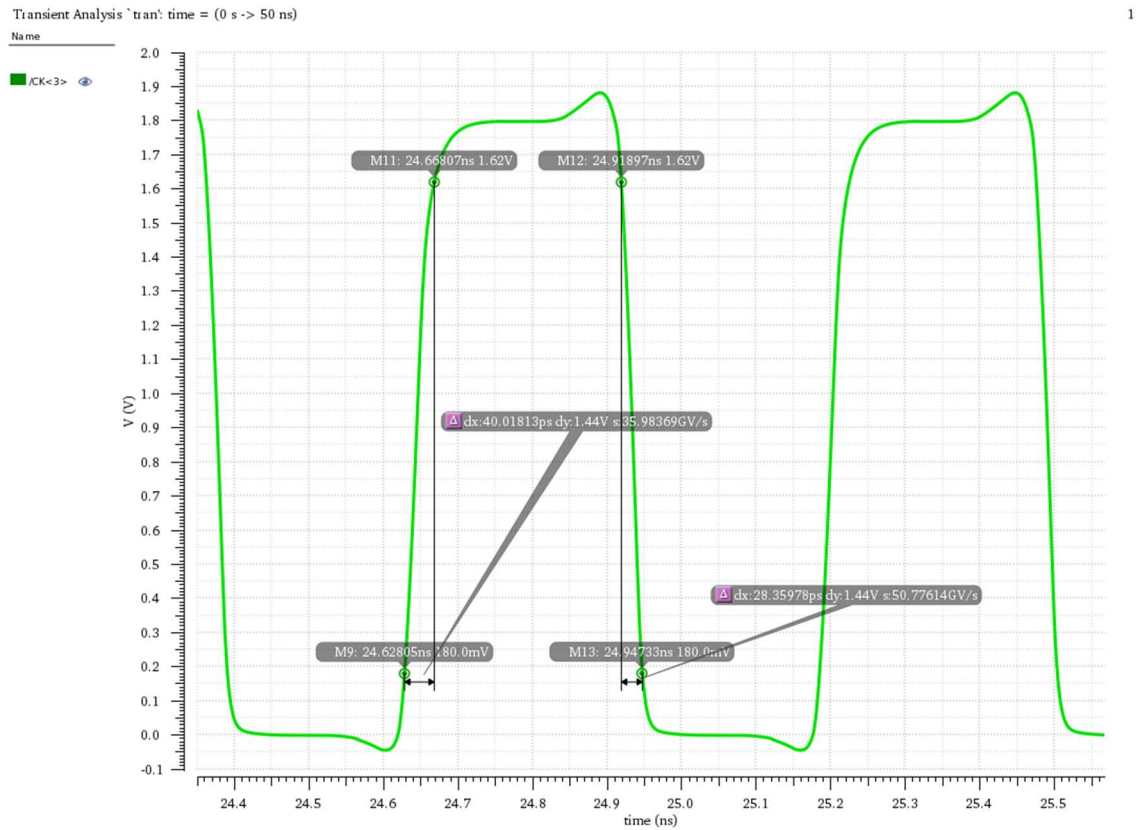**Figure 4.2**: The period of the designed ring oscillator output

Figure 4.3: The rise and fall time of the designed ring oscillator output.
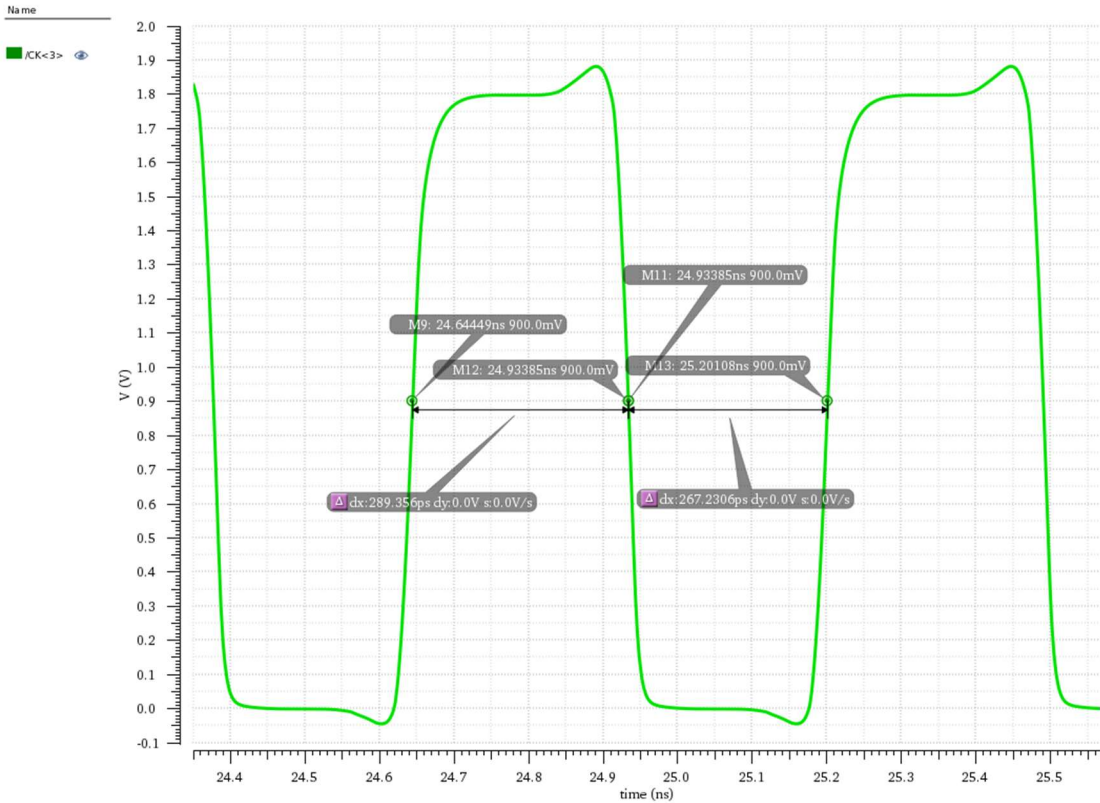
Figure 4.4: The duty cycle of the designed ring oscillator output.

4.2. Coarse Tuning Part

In this work, A 16x16 DCR is proposed where the resistance value of R is selected to be equal to 166 Ω. It is constructed using PMOS devices only in order to reduce the current drained into the circuit as well as the occupied size of the design compared to when NMOS devices are added as well. The designed DCR uses an 8-bits control code where the Most Significant Bits (MSB) are used for the row resistors control and the Least Significant Bits (LSB) are used for the column resistor control. Thus, 8-bits control code is divided into 4-bits MSB for row control and 4-bits LSB for column control. Hence for a AxB DCR as shown before, A is 2^{MSB} and B is 2^{LSB}. **Table 4.2** shows the chosen parameters of the first column resistor devices. **Table 4.3** is the parameters of the row resistors excluding the first column devises. The proposed work is capable of tuning the ring oscillator in the range of (278.9MHz - 1.14GHz) with a frequency step of 1.9MHz at 400MHz and 3.8MHz at 560MHz as depicted in **Figure 4.5** and **Figure 4.6**. **Table 4.4** provides the achieved coarse tuning range using the designed DCR.

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Table 4.2: The parameters of the first column resistor devices.

1st column	Finger Width (μm)	Finger Count	Multiplier	Total Width of 2R device (μm)	Total Width of R device (μm)	Length (μm)
PMOS	3.5	10	1	35	70	0.18

Table 4.3: The parameters of the row resistor excluding the first column devises.

Row resistors	T1	T2	T3	T4	T5	T6	T7	T8	Total Width
Number of fingers	1	1	1	1	2	2	2	2	
Width (μm)	1	1	1	1	2	2	2	2	
Row resistors	T9	T10	T11	T12	T13	T14	T15	T16	
Number of fingers	2	2	2	3	3	3	4	4	35 μm
Width (μm)	2	2	2	3	3	3	4	4	

Table 4.4: The achieved coarse tuning results in the typical corner.

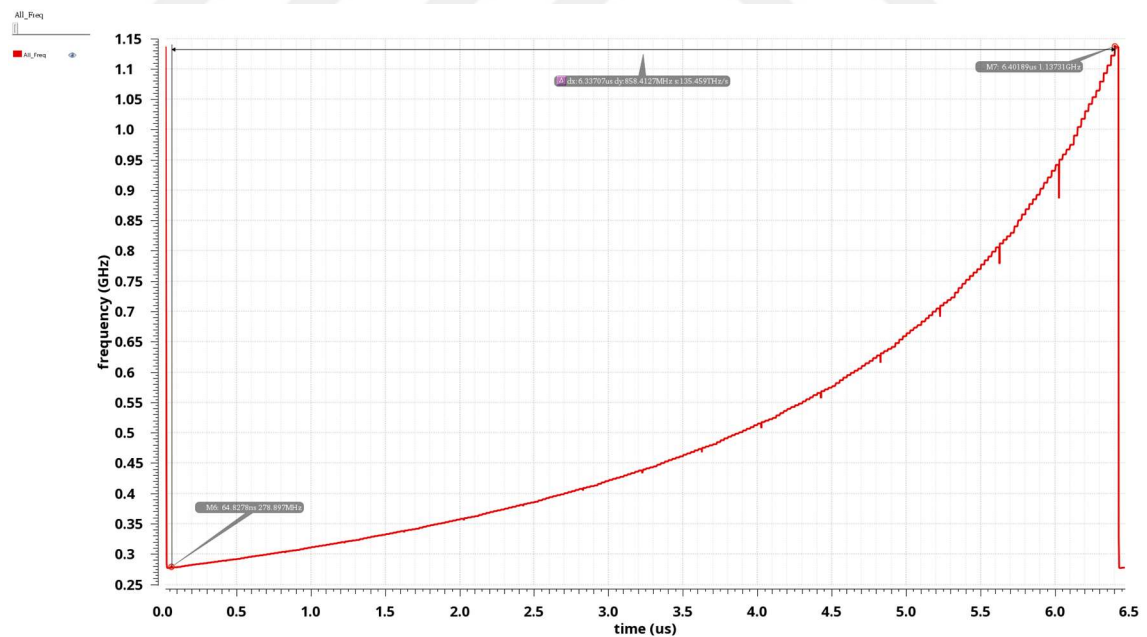| Coarse Tuning Ranges	Lowest Frequency	Highest Frequency	Step at 400MHz	Step at 560MHz	Minimum step	Maximum step
	278.9MHz	1.14GHz	1.9MHz	3.8MHz	593KHz	15.9MHz

Figure 4.5: Full tuning range of the proposed DCR.
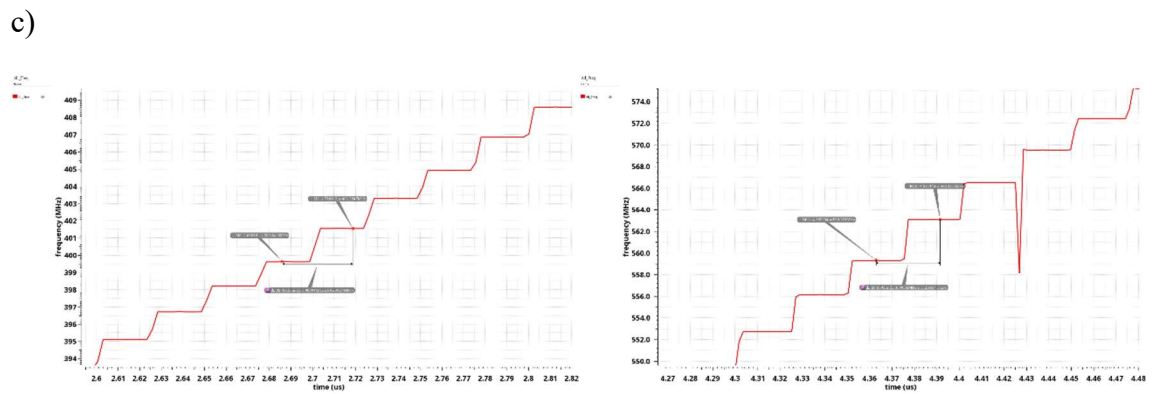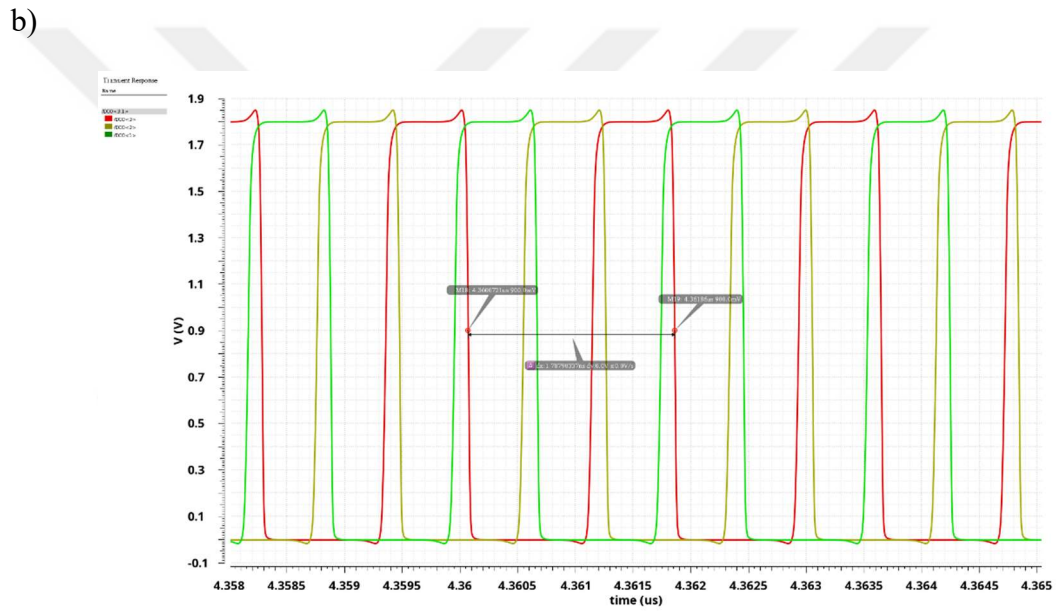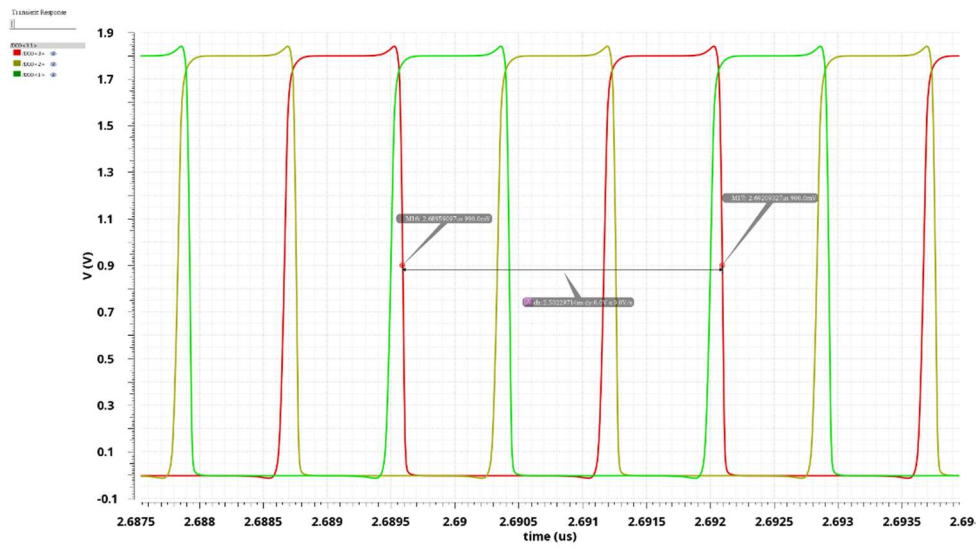
a)

33

Figure 4.6: The oscillation waveform and steps; **a)** Waveform at 400MHz. **b)** Waveform at 560MHz. **c)** Steps at 400MHz and 560MHz.

4.3.   Fine Tuning Part

An 8-bits control code is divided into 5-bits for the resistor ladder and 3-bits for the switched capacitor array in order to reduce the spur noise introduced by the transition stages of the switched capacitor array. The 5-bits resistor ladder is built up with a set of 32 cascaded resistors. The total resistance of the resistor ladder is equal to 3.2kΩ with a step of 100Ω resistance providing a voltage step of 56mV since the supply voltage is 1.8V. The equivalent capacitance of the switched capacitor array is 2pF, which is divided into 8-steps of 250fF capacitance step. The selected varactor device has a tuning range of 15.5fF from 10.8fF to 26.3fF. The varactor tuning range at 400MHz and 560MHz are shown in **Figure 4.7** and **Figure 4.8**. **Table 4.5** demonstrates the parameters used to design the varactor device and the corresponding tuning range achieved. **Table 4.6** shows the voltage and the frequency steps accomplished by the resistor ladder and the switched capacitor array. Finally, **Table 4.7** presents the achieved results of the proposed fine tuning.

Table 4.5: The parameters of the varactor device.

Varactor Parameters	Device Width	Device Length	Capacitance Range	Frequency Range
	2 μm	2 μm	15.5fF	20MHz

Table 4.6: The voltage and the frequency steps of the RC DAC.

Design Resolution	Resistance Step	Capacitance Step
Voltage	56V	7mV
Frequency	0.30MHz	37KHz

Table 4.7: The achieved fine-tuning results in the typical corner.

Fine Tuning Ranges	Range at 400MHz	Step at 400MHz	Range at 560MHz	Step at 560MHz	Lowest Range	Highest Range
	10MHz	37KHz	13.9MHz	52KHz	5.5MHz	20MHz

a)

b)
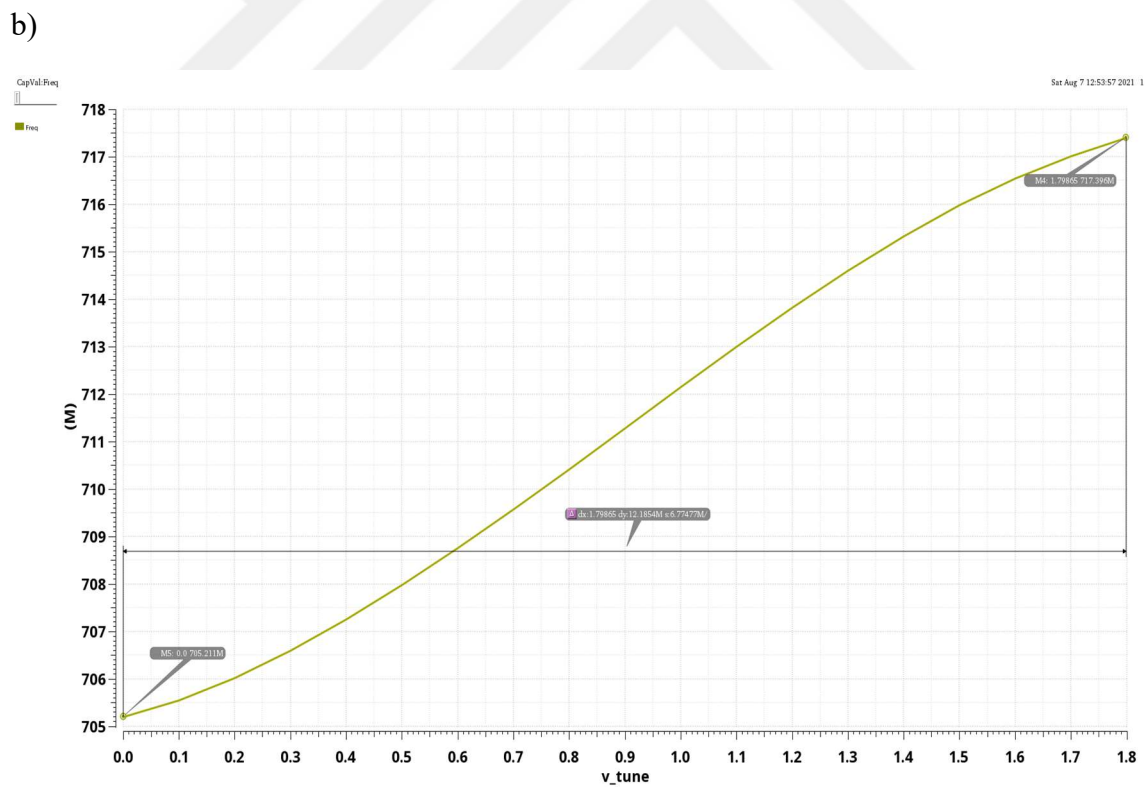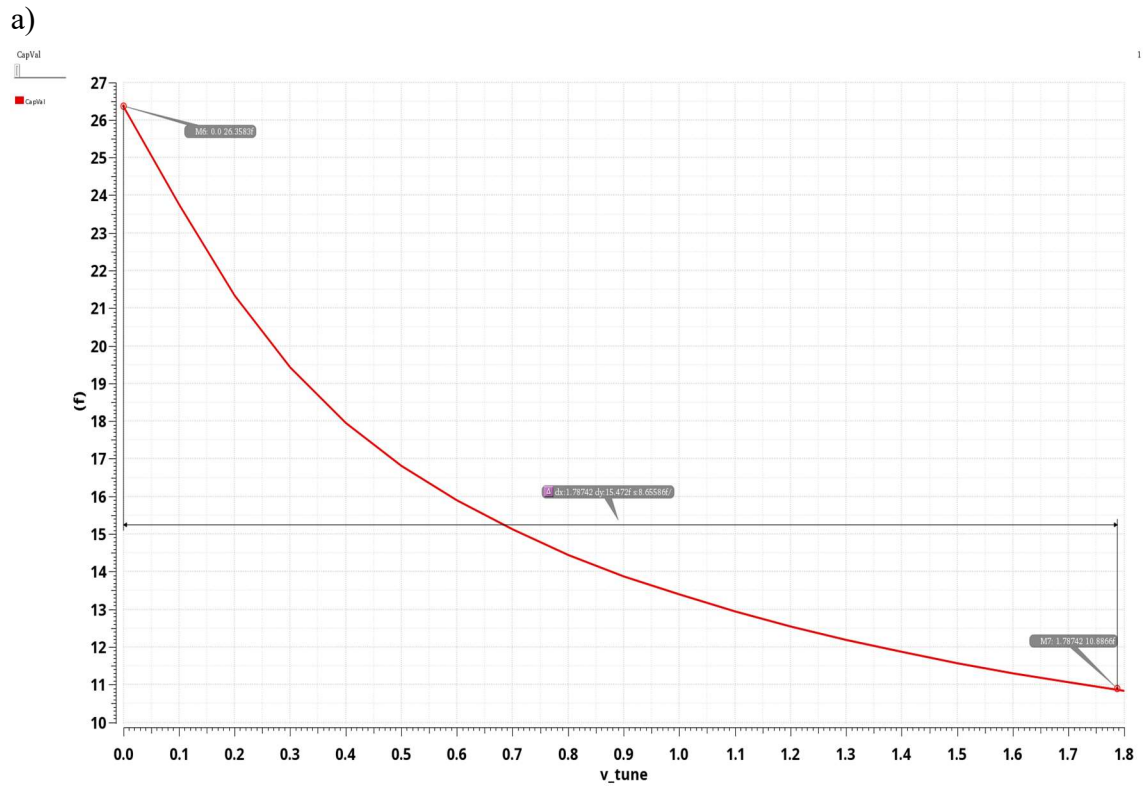
Figure 4.7: Varactor performance. **a)** The capacitance changes as the supply voltage changes. **b)** The frequency changes while the capacitance of the varactor changes.

a)
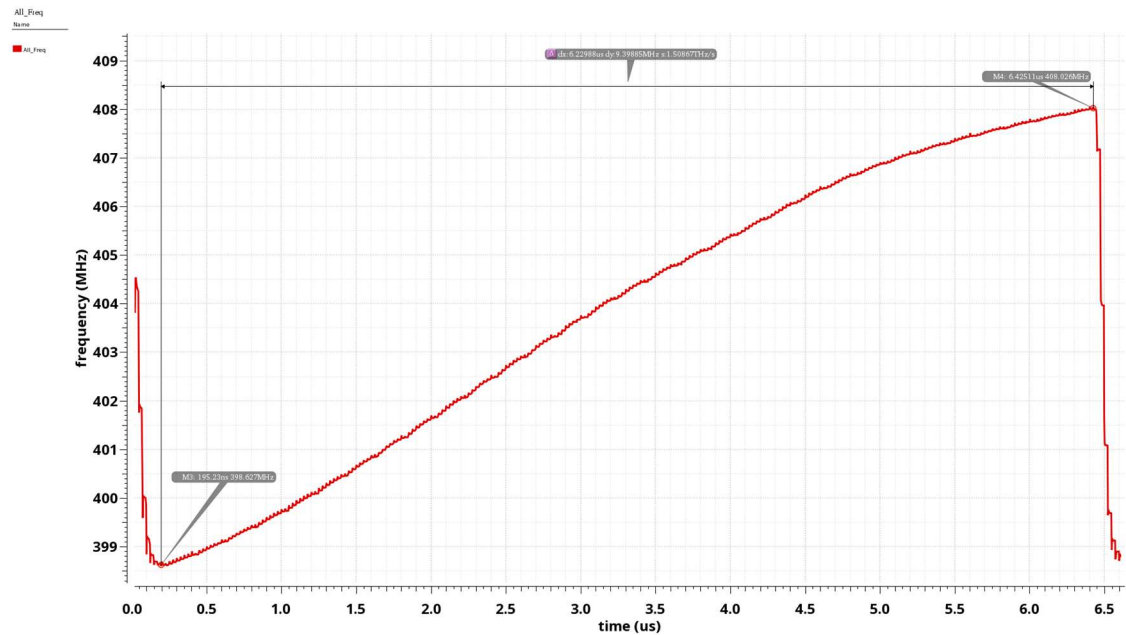
b)
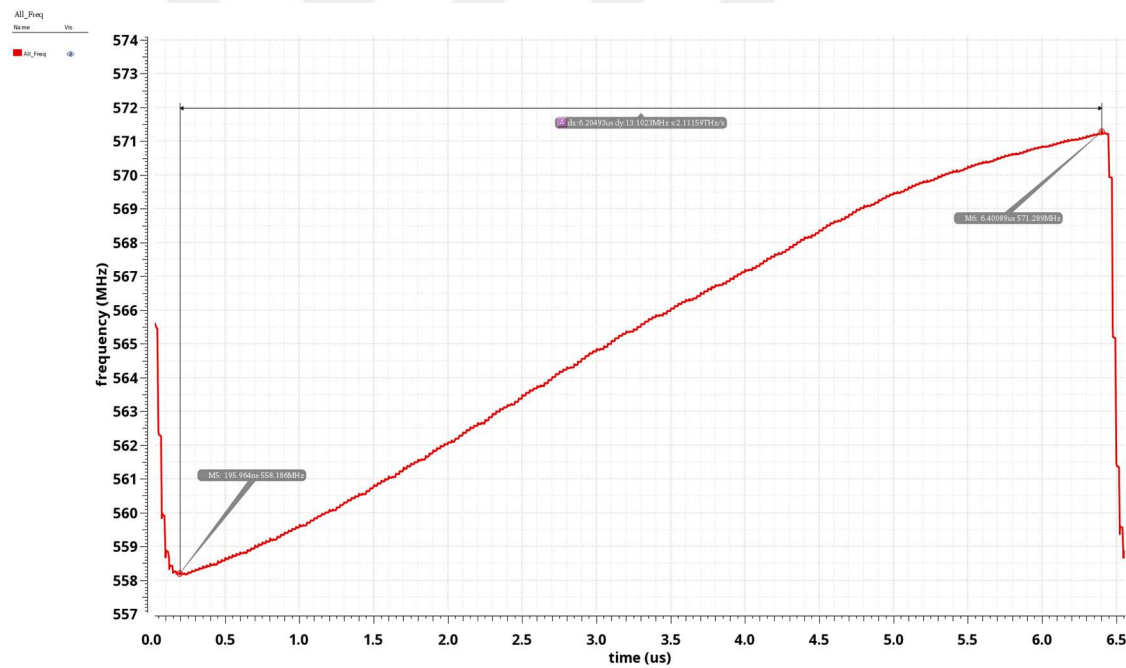
Figure 4.8: Fine tuning performance. **a)** Achieved fine range at 400MHz. **b)** Achieved fine range at 560MHz.

4.4. Process Corner Tuning Part

The proposed switched capacitor array uses 3-bits code and contains 8 parallel 50fF capacitors resulting in overall of 400fF additional load capacitance. The fundamental purpose of using all these tuning methods is to ensure that the DCO oscillation

frequency range covers 400MHz and 560MHz for all PVT cases. **Table 4.8** below shows the performance of the proposed DCO for all PVT cases.

Table 4.8: DCO performance for all PVT cases.

400MHz /560MHz	Temperature	1.62V		1.8V		1.98V	
		Min freq (MHz)	Max freq (MHz)	Min freq (MHz)	Max freq (MHz)	Min freq (MHz)	Max freq (MHz)
WS	71º	195	787	207.7	830.3	260	824
	27º	215	740	213.6	883.3	263	845
	-40º	214	761	224.1	983.9	274	900
TM	71º	242	782	275.4	1070	292	882
	27º	237	779	278.9	1014	294	890
	-40º	238	780	296.4	1252	300	893
WP	71º	263	800	294	850	359	949
	27º	244	784	297	857	366	956
	-40º	228	890	300	1070	350	1400

WS is worst speed (slow process),

TM is typical environment,

WP is worst power (fast process).

4.5. Noise and Power Consumption.

Noise performance and power consumption are two critical metrics in oscillation design. Thus, in order to check the overall performance of the proposed DCO design, it is required to test the noise and power performance in addition to the tuning tests discussed in the previous sections. The amplitude of the DCO output is 1.8V as it is a full rail-to-rail waveform. The current passing through the proposed DCO including RO and all tuning parts is measured for the oscillation frequencies of 400MHz and 560MHz. The current values are 1.59mA and 2.13mA respectively. **Figure 4.9** and **Figure 4.10** show plots of the current waveform in the DCO when oscillating at 400MHz and 560MHz respectively.
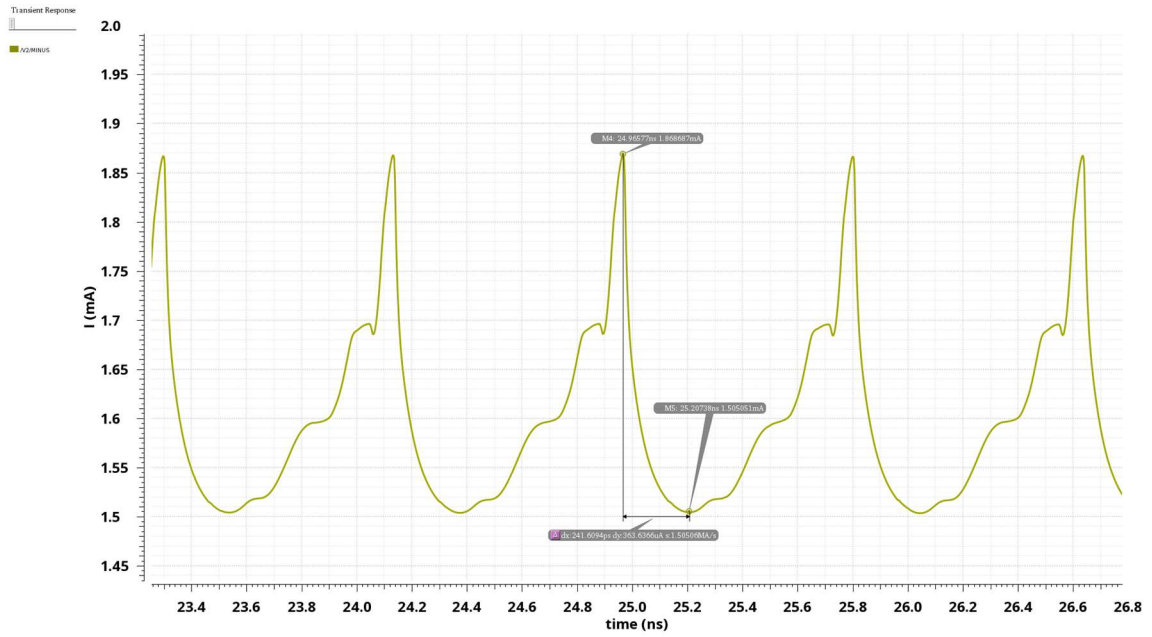
Figure 4.10: The current fluctuation at 400MHz oscillation.
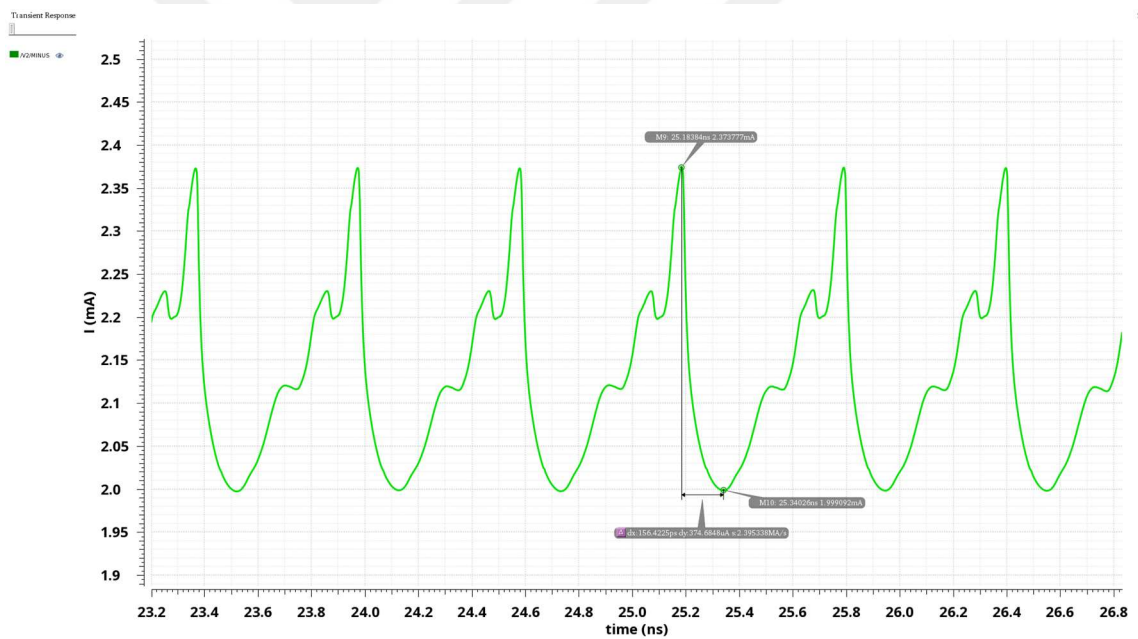
Figure 4.9: The current fluctuation at 560MHz oscillation.

Phase noise performance is depicted in **Figure 4.11** and **Figure 4.12** at 400MHz and 560MHz oscillation frequencies. The phase noise is shown at 1MHz offset for both main core oscillation frequencies (400MHz – 560MHz). The phase noise is -113.9dBc and -111.8dBc for 400MHz and 560MHz respectively. The phase noise and power performance summary are provided in **Table 4.9.**

Table 4.9: DCO noise and current performance summary.

	Current Flow	Phase Noise @ 1MHz	Power Consumption
400MHz	1.59 mA	-113.9 dBc	2.86mW
560MHz	2.13 mA	-111.8 dBc	3.83mW
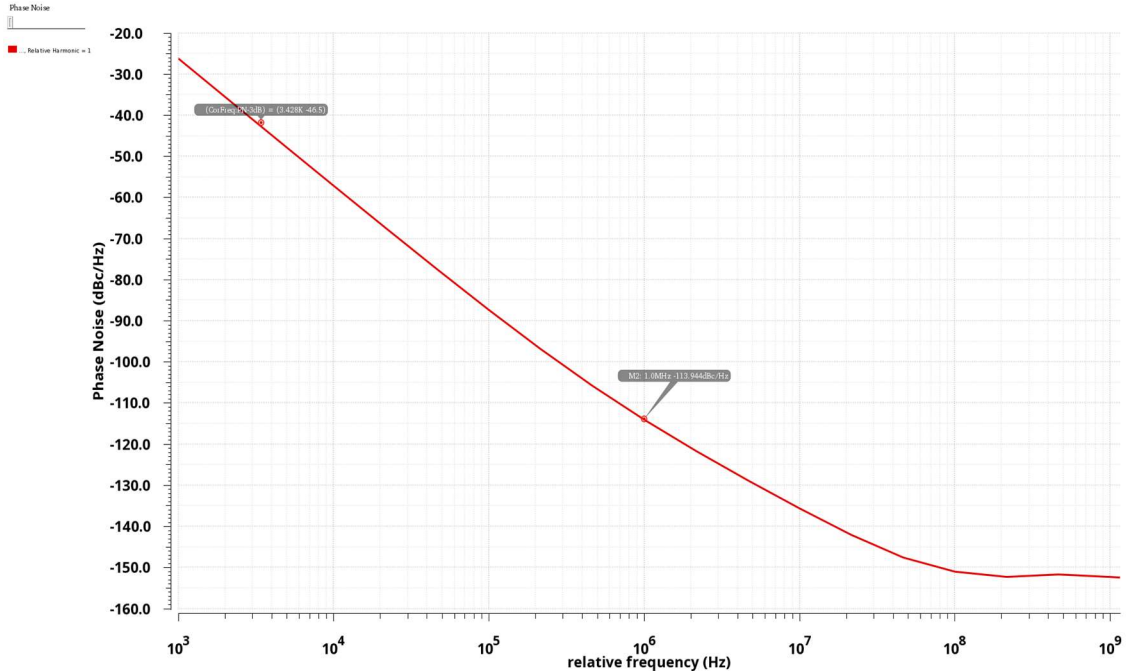
Figure 4.11: Phase noise at 400MHz oscillation.
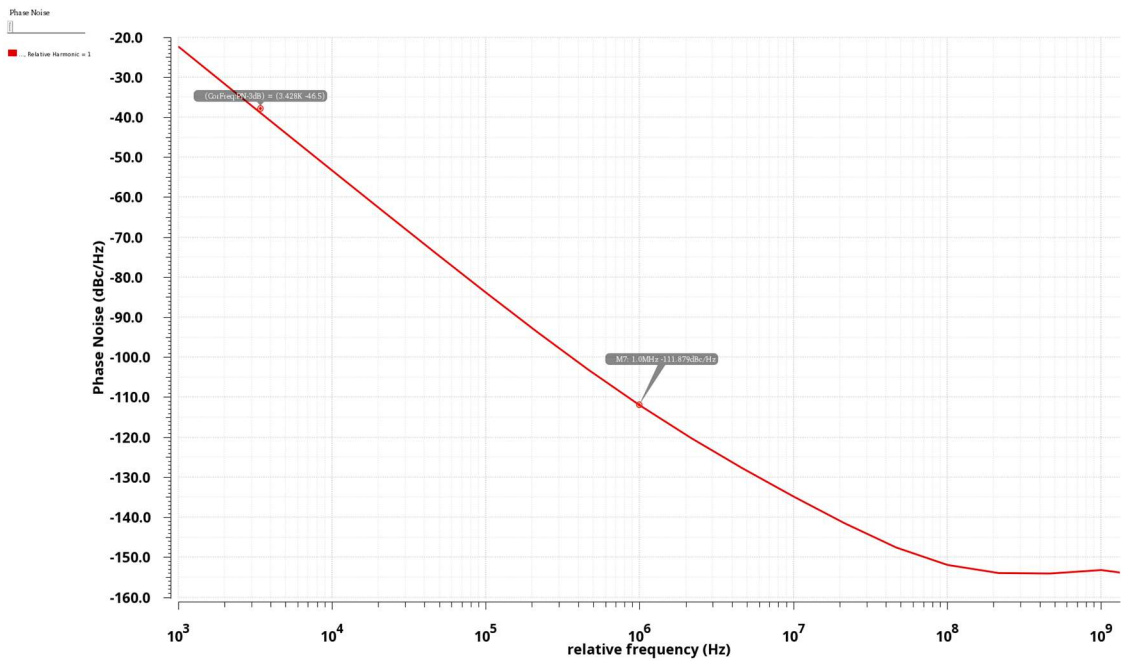
Figure 4.12: Phase noise at 560MHz oscillation.

4.6. Layout Design and Post-Layout Simulations.

4.6.1. Layout summary

This design in this work is implemented using XH018 0.18μm CMOS technology. The layout design was done using Cadence Virtuoso Layout editor tool, where five metals layers were used to construct the layout of the proposed DCO. **Figure 4.13** shows the Top-Level layout design of the DCO including all sup-blocks and parts. The overall layout dimensions are 245μm in width and 315μm in height, where **Table 4.10** presents a summary of all DCO part sizes.

Table 4.10: DCO Layout summary.

	Name of Block	Size in Micron (Width/Hight)	Number of Blocks
Digital Blocks	3to8 Decoder	25x30	2
	4to16 Decoder	25x60	2
	5to32 Decoder	25x140	1
	Buffer	6x5	4
	16-bits Register	36x51	2
	32-bits Register	36x95	1
	8-bits Register	36x30	1
Main Blocks	Corner Cap Array	31x78	1
	Fine Ctrl	145x86	1
	PMOS DCR	50x155	1
	DCR Ctrl	126x167	1
	RO	32x37	1
DCO Top-Level Dimensions		245μm x 315μm	
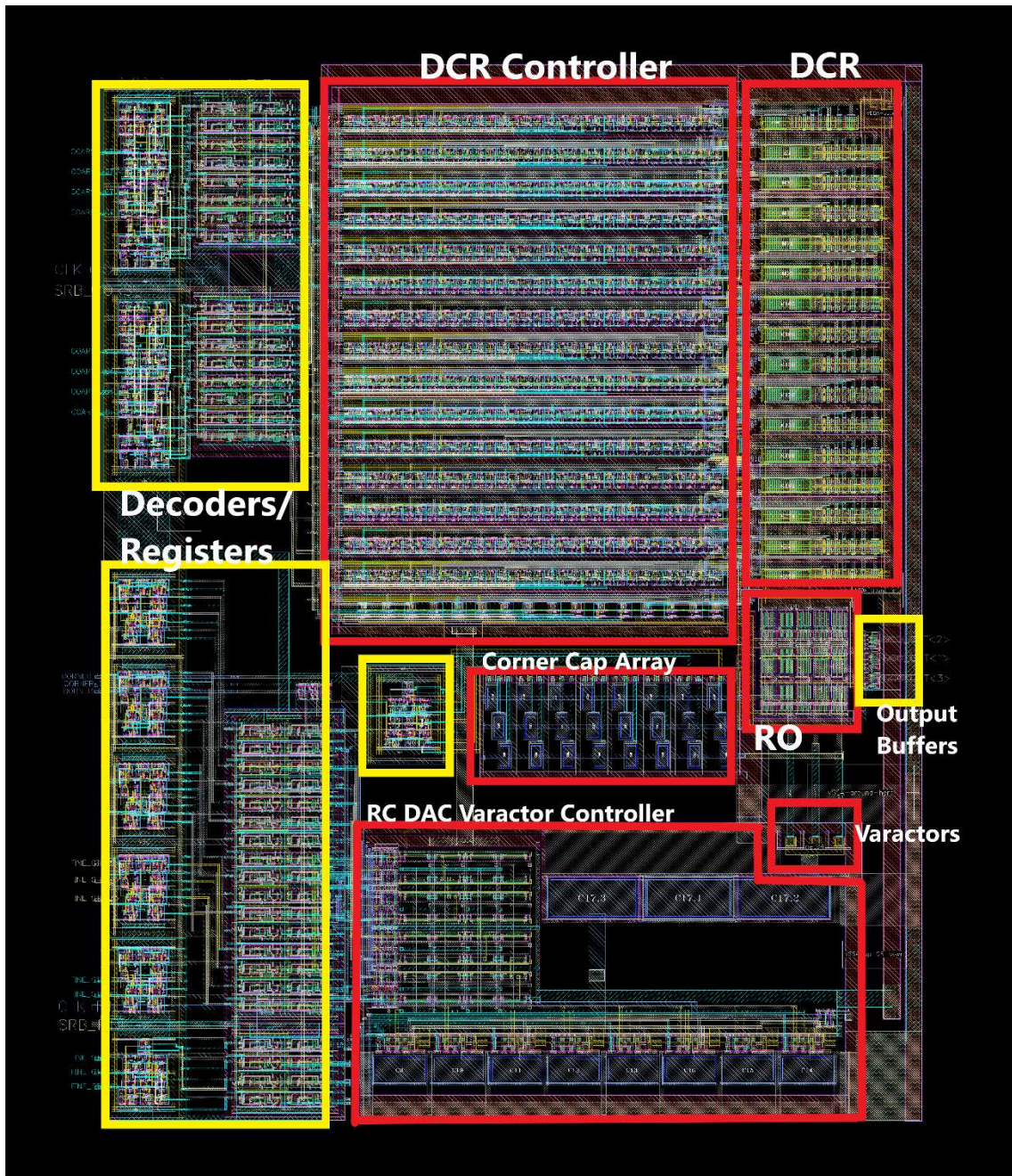
Figure 4.13: DCO Top-Level Layout design.

4.6.2. Post-layout simulations

One of the significant issues that degrade and limit the performance of the design is the effect of the layout parasitics. Layout parasitics are mainly unwanted capacitance and resistance due to the wiring and the metals of the devices. Hence, parasitic extraction is done for each block of the proposed DCO and all the coarse tuning, fine tuning and PVT cases are checked again. **Table 4.11** summarizes the results of the post-layout simulations.

Table 4.11: DCO Post-Layout Simulations Results.

	Typical Simulations	Post-Layout Simulations
Coarse Tuning Range	278.9MHz / 1.14GHz	261.6MHz / 1.07GHz
Fine Tuning Range at 400MHz	10MHz	9.3MHz
Fine Tuning Range at 560MHz	13.9MHz	13MHz
Slowest Corner (71º,1.62V, WS)	195MHz / 787MHz	182MHz / 724MHz
Fastest Corner (-41º,1.98V, WP)	350MHz / 1.4GHz	335.6MHz /1.37GHz

4.7. Performance Comparison

In order to summarize this work and compare with other state-of-the-art published designs, **Table 4.12** is introduced.

Table 4.12: Performance Comparison.

Reference	[16]	[15]	[4]	This Work
Technology	180nm	180nm	180nm	180nm
Tuning Range	316MHz / 1.165GHz	523MHz / 2.11GHz	310MHz / 680MHz	278.9MHz / 1.14GHz
Supply Voltage	1.8V	2V	0.8V	1.8V
Power Consumption	23.18mW	14.8mW	0.32mW	2.86mW
Phase Noise	-114.6dBc	-103.3dBc	-100.8dBc	-113.9dBc
Architecture	Ring	Ring	Ring	Ring

CHAPTER 5

5.   ARTIFICIAL INTELLIGENCE MODEL OF THE DCO

Due to the gap between theory and real design environment, applying the equations directly is still missing some parameters such as the used technology and the parasitic caused by the routing metals and wiring that degrade the desired results. In this section, a Neural Network (NN) model that predicts the frequency value for the given DCO parameters with respect to the environment and technology of this work, is studied.

5.1.   Introduction

In this NN model, the dataset is extracted from the proposed DCO design using XH018 0.18μm CMOS technology. This dataset consists of two main features, resistance values and the capacitance values. The output data is the oscillation frequency values of the designed DCO. The significance of these features is that they are the key parameters for tuning the oscillation frequency.

A single-hidden layer neural network model based on backpropagation algorithm is prepared to predict the oscillation frequency of an DCO giving the resistance and capacitance parameters. The prepared NN model is capable of predicting the oscillation frequency of a VCO effectively based on XH018 0.18μm CMOS technology including noise effects and the parasitics produced at layout level. The type of the training model used in this work is called regression training model, which is used in predicting the continuous output (integer or decimal values) of a system based on the relation between the inputs and the outputs of the system.

5.2.   Method and Theory

The dataset is exported form Cadence environment and applied on MATLAB software where the modelling part takes the place. The model training and testing process are

performed using MATLAB platform. The performance of the designed model was measured using the mean square error (MSE) as **(4.1)**;

$$MSE = \frac{1}{N} \sum_{i=0}^{N-1} (r - y)^2 \tag{4.1}$$

where r and y are desired output and predicted output of the NN model, respectively, and N denotes number of instances.

Two approaches are applied in order to find the best match for this data.

1- Single Layer Perceptron:

A Single Layer Perceptron is created based on the provided inputs and outputs, then start learning in an attempt to reach convergence. In single layer perceptron, the output of the regression model is a weighted sum of the inputs **(4.2)**;

$$y = w^T x \tag{4.2}$$

which is valid just in case the output is a linear function of the inputs, In the case of this project, the dataset cannot be fit into a linear model due to the due to the scale and variation in the features. Thus, the single layer perceptron network failed to achieve convergence and the network reach a very high error [28].

2- Multilayer Perceptron:

In Multilayer Perceptron approach, one hidden layer is selected for the model with the sigmoid function for the hidden unit outputs when there is no activation function for the output layer since the prediction is for a regression model. The equation of the sigmoid and linear function of any input x in hidden layer and output y in output layer are given as **(4.3)**;

$$f(x) = \frac{1}{1 + e^{-x}} \tag{4.3}$$

The model applies online learning, in which the error is calculated for individual instances, not over the whole samples. Starting from random initial weights, at each iteration, the parameters are adjusted a little bit to minimize the error, while keeping what the model has previously learned [28].

5.3.   Discussion and Results

The dataset is shown in **Figure 5.1** and it is organized so that in each resistance step, all the capacitance steps are swapped which represents the operation of the coarse and the fine tuning of the DCO. The data then shuffled randomly to ensure that each data point creates an independent change on the model. It is divided into two parts; train data and validation data with the proportion of 7.5:2.5. Since the data is shuffled, the first 75% and the second 25% of the datasets are selected as a training set and the test set, respectively. The data consists of impulsive changes due to the large variation between the frequency unit scale and the capacitance unit scale. Therefore, larger values overshadows the smaller values, and the model fails to fit the data properly. In order to prevent this problem and to have an efficient neural network training process, the dataset is normalized to fit in the range of [-1, 1] [29].

The training process is done multiple times by using a different number of hidden units across the number of epochs where the number of hidden units starts at 1 and goes up to 15 hidden units with a maximum number of 100,000 epochs. This is done to achieve the best number of hidden units which is chosen using the cross-validation and checking Mean Squared Error (MSE) graph for each trail. **Figure 5.2** shows the errors rate decrease from first epoch until the learning reaches last epoch. The best MSE for both training and test dataset is achieved using 5 hidden neurons for around 930 epochs. The Learning Factor (LF) is changed throughout the training process iterations in order to find the best learning factor that makes all the weights to converge. It starts at 0.025 and goes up to 0.9 where the best LF is found to be 0.25. **Figure 5.3** depicts the convergence of the synaptic weights for the hidden units in the training prosses where **Figure 5.4** shows the same but for the output layer. The initial synaptic weights for the whole training process for both input layer and output layer were between -0.01 and 0.01 chosen from uniformly distributed values. The performance of the NN model gives promising results predicting the oscillation frequency with an average error of 2.5MHz, where MSE is 3.95×10^{-5} and Root Mean Squared Error (RMSE) is 0.0063. **Figure 5.5** and **Figure 5.6** are plots comparing the actual output that the model predicts for frequency values and the desired output that is provided from the proposed DCO design results. It is clearly seen in the plots and the performance of the model that both values are matching meaning that this ANN model is predicting the output frequency of the DCO effectively for the given resistance and capacitance value. This studied approach

narrows down the gap between theory and real design environments and reduces the required design time expanding the horizon of new design methodologies and breaking the limitations of analog circuit design automation.
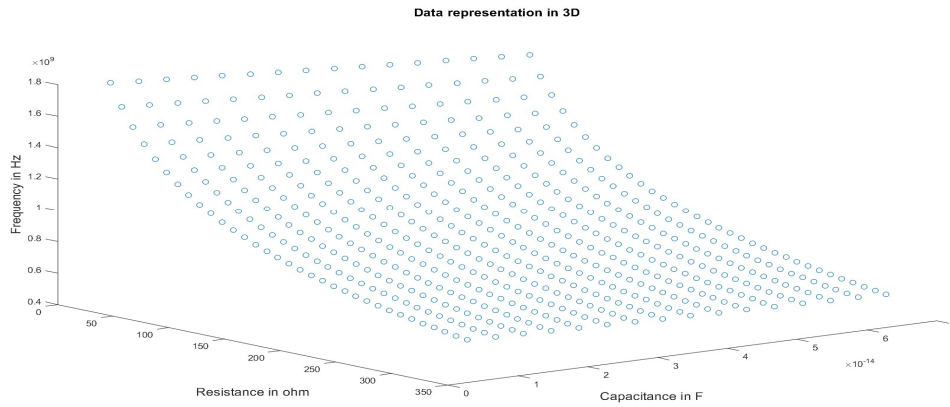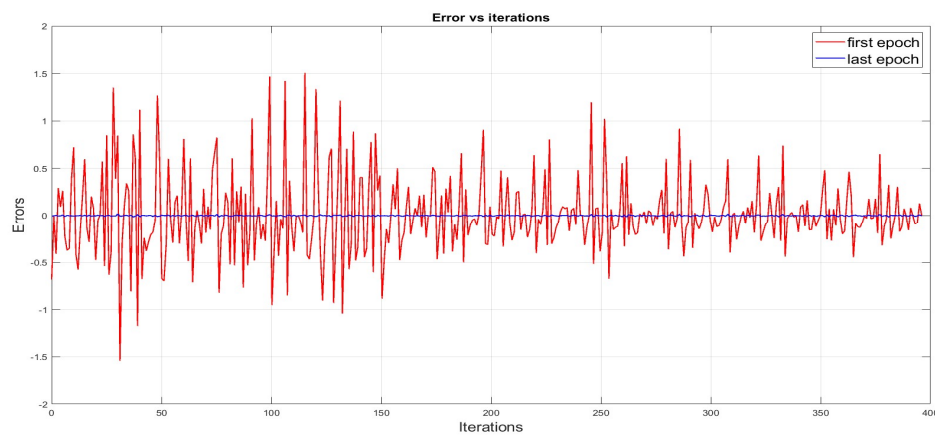

Figure 5.1: The dataset visualization in 3D.

Figure 5.2: Errors rate at first epoch and last epoch.
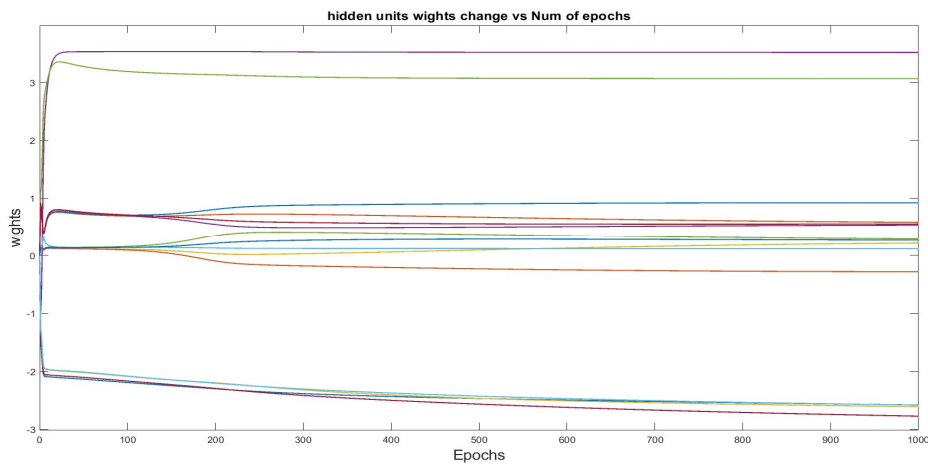

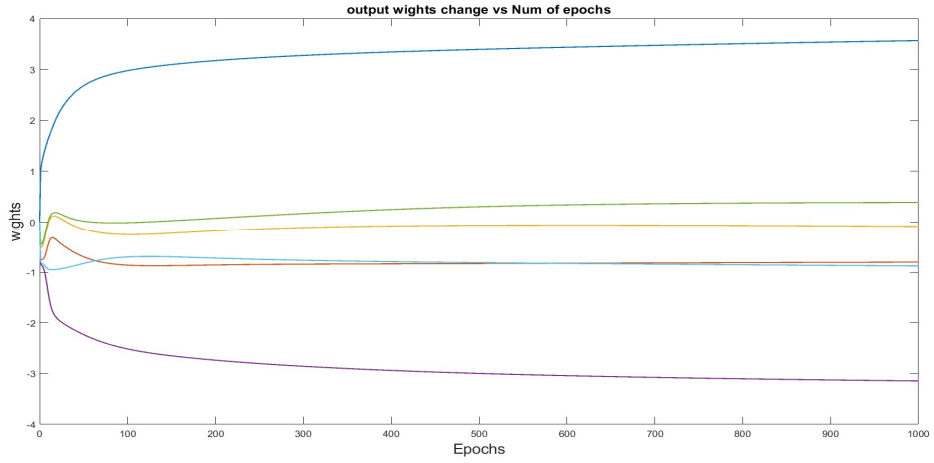**Figure 5.3:** The synaptic weights convergence for hidden units.

47

Figure 5.4 : The synaptic weights convergence for output layer.
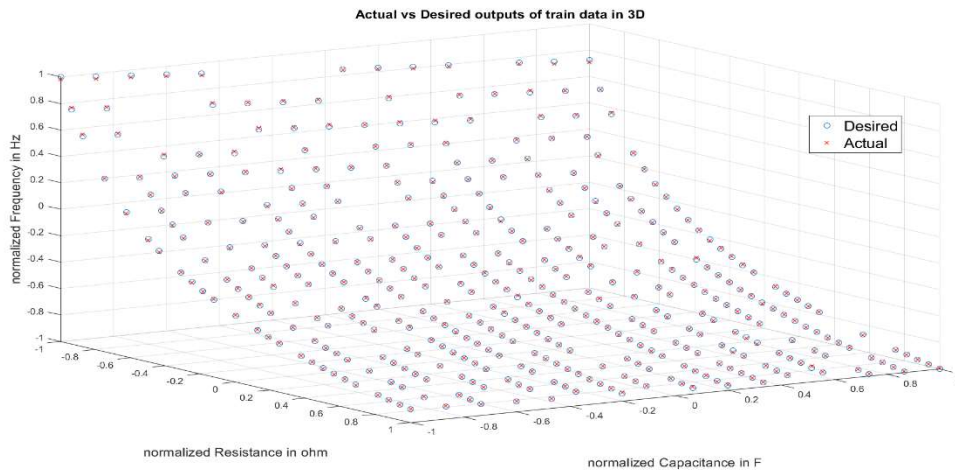

Figure 5.5: The comparison of the model prediction with the proposed DCO output for training data part.
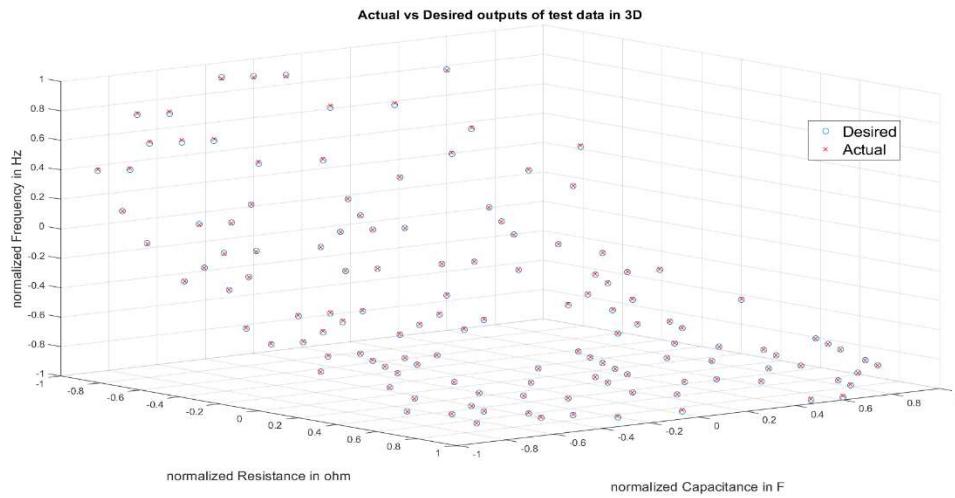

Figure 5.6: The comparison of the model prediction with the proposed DCO output for test data part.

CHAPTER 6

6. CONCLUSIONS AND FUTURE WORK

PLLs are one of the critical blocks used for RF carrier and clock generation in communication applications, RF/ analog, and digital circuits. PLLs require oscillators to generate and deliver the oscillation waveform. Oscillators are considered to be essential components to study and develop due to their precious functionality in generating waveforms ranging from low-frequencies to high-frequencies as desired. The work in this thesis presents a digitally controlled ring oscillator with a sufficiently wide tuning range and fine resolution tuning steps. The designed DCO is based on single-ended ring oscillator topology since it is dedicated to ADPLL and guarantees a wide tuning range with as small area as possible. A single-ended ring oscillator is selected due to the power efficiency advantage of the structure and it provides a full swinging output signal. It consists of three cascaded stages where each stage is built up by five parallel units to ensure the strength of the output signal.

In order to obtain a sufficiently wide tuning range with fine resolution steps and to cover the PVT corners, the design relies on three main tuning approaches for coarse tuning, fine tuning and process corner tuning. An 8-bits DCR is designed for coarse tuning since it gives relatively big tuning steps in order to cover a wide tuning range. Due to coarse tuning, this work is capable of tuning the DCO in the range of (278.9MHz - 1.14GHz) with a frequency step of 1.9MHz at 400MHz and 3.8MHz at 560MHz. To obtain a wide tuning range and fine resolution steps simultaneously, fine-tuning, which is based on an 8-bits digitally controlled RC DAC that controls the varactor load at the output of the ring oscillator is also proposed. The fine-tuning network covers the desired range with 37kHz frequency step. 3-bits switched capacitor array is introduced to mitigate the degradation in the overall performance of the DCO due to Process, Voltage, and Temperature changes (PVT). The PVT corner covered are

10% voltage change, the temperature range of (71º, - 40º), and the change in the technology speed as slow, typical, and fast.

The main supply voltage for this work is 1.8V, thus it is the amplitude of the DCO output as full rail-to-rail waveform. The current in the DCO at 400MHz and 560MHz is 1.59mA and 2.13mA respectively. The phase noise is -113.9dBc and -111.8dBc for 400MHz and 560MHz respectively at 1MHz offset for both main core oscillation frequencies. This work was done on Cadence Virtuoso using XH018 0.18μm CMOS technology from XFAB. The layout was done with five metal layers and the overall layout dimensions are 245μm in width and 315μm in height.

In this work, an artificial neural network-based model is proposed in order to cover the gap between theory and the real design environment and to reduce the required design time. The dataset used for training and testing the model is extracted from the designed DCO outcome. The performance of the NN model gives promising results predicting the oscillation frequency with an average error of 2.5MHz, where the Mean Squared Error (MSE) is 3.95×10^{-5} and Root Mean Squared Error (RMSE) is 0.063.

The studies and works achieved in this thesis gave promising results taking into consideration the older 0.18μm CMOS technology used. However, for future research and development in the field of DCO design, it is still important to present the following recommendations;

- Although the proposed design fits within dimensions of 245μm by 315μm, the 0.18μm CMOS technology limits the design size. Future work will be using advanced newer CMOS technologies.
- In designing the top-level layout, the parasitic of all blocks was extracted and thus simulations were made multiple times to guarantee the performance of the designed DCO. However, it requires more effort while designing the top-level layout, and more attention on the bond wires and pads should be given.
- The current consumption is around 1.59mA and 2.13mA due to the resistive load used for tuning the DCO. An alternative tuning method can be introduced in the future for better power performance.
- Despite the unique approach to model the DCO, the model still needs to be improved by providing more datasets for a wider frequency range and more accurate performance.

- Indeed, more parameters can be considered while modeling the DCO as it was only capacitance and resistance load for the case of this work.

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PUBLICATIONS, PRESENTATIONS, AND PATENTS ON THE THESIS:

- H. Mousa, O. Hamzeh, M. H. Mahmoud and I. Cicek, "A Machine Learning Based Autonomous Drone Navigation Assistance System for Indoors," *Electrical and Electronics Engineering Conference (ELECO),* November, 2018, Turkey.

DESIGN OF A DIGITALLY CONTROLLED RING OSCILLATOR FOR ADPLL