A HIGH-RESOLUTION TIME TO DIGITAL CONVERTER DESIGN FOR ALL DIGITAL PHASE-LOCKED LOOPS

A THESIS SUBMITTED TO
THE GRADUATE SCHOOL OF
ENGINEERING AND NATURAL SCIENCES
OF ISTANBUL MEDIPOL UNIVERSITY
IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR
THE DEGREE OF
MASTER OF SCIENCE
IN
ELECTRICAL, ELECTRONICS ENGINEERING AND CYBER SYSTEMS

By

Tamer Eren

June, 2021

A HIGH-RESOLUTION TIME TO DIGITAL CONVERTER DESIGN FOR ALL DIGITAL PHASE-LOCKED LOOPS

By Tamer Eren

30 June 2021

We certify that we have read this dissertation and that in our opinion it is fully adequate, in scope and in quality, as a dissertation for the degree of Master of Science.

_____

Assoc. Prof. Dr. Hakan Doğan (Advisor)

_____

Assoc. Prof. Dr. Tufan Coşkun Karalar

_____

Assist. Prof. Dr. Hüseyin Şerif Savcı

Approved by the Graduate School of Engineering and Natural Sciences:

_____

Assoc. Prof. Dr. Yasemin Yüksel Durmaz

Director of the Graduate School of Engineering and Natural Sciences

I hereby declare that all information in this document has been obtained and presented in accordance with the academic rules and ethical conduct. I also declare that, as required by these rules and conduct, I have fully cited and referenced all material and results that are not original to this work.

Signature :

Name, Surname: TAMER EREN

ACKNOWLEDGEMENT

The completion of this master thesis could not have been possible without the significant assistance of so many people around me. Unfortunately, enumerating them impossible because of limitations but their contributions are gratefully appreciated.

Before anyone, I submit my heartiest gratitude to Assoc. Prof. Hakan DOĞAN, who shared and taught me everything about this field expertly. I also owe him a lot, for his patience and tolerance for my endless and timeless questions.

Another person I cannot continue without expressing my high gratitude to is Dr. Mustafa AKTAN. Whenever I tried to solve any problem during the thesis, he instantly helped me without hesitation. His guidance through this project is incomparable to anyone else.

Also, my teammate, Zehra Nur OKTAY deserves special thanks for her motivations for maintaining a positive atmosphere during the research and for being a very good support for me in every difficult situation.

Finally, I would like to serve my deep gratitude to my mom, wife, and family for their countless and immeasurable contributions from the beginning of my education.

This thesis was funded by ASELSAN

Tamer Eren

June, 2021

CONTENTS

Page

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

μ : Micro
Ω : Resistance
f : Frequency
Hz : Hertz

ABBREVIATIONS

PLL : Phase-Locked Loop
TDC : Time to Digital Converter
PET : Positron Emission Tomography
INL : Integral Nonlinearity
DNL : Differential Nonlinearity
TOF : Time of Flight
FLIM : Fluorescence Lifetime Imaging
TOFMS : Basics of Time-of-Flight Mass Spectrometry
LiDAR : Light Detection and Ranging
VCO : Voltage Controlled Oscillator
PD : Phase Detector
PFD : Phase Frequency Detector
DCO : Digitally Controlled Oscillator
RO : Ring Oscillator
DAC : Digital to Analog Converter
ADC : Analog to Digital Converter
ECG : Electrocardiogram
SSCG : Spread Spectrum Clock Generation
ADPLL : All Digital Phase-Locked Loop
DPLL : Digital Phase-Locked Loop
SPLL : Software Phase-Locked Loop
RF : Radio Frequency
FPGA : Field Programmable Gate Array
AI : Artificial Intelligence
SAR : Successive Approximation
TA : Time Amplifier
NMOS : Negative-Channel Metal Oxide Semiconductor
PMOS : Positive-Channel Metal Oxide Semiconductor
ASCI : Application Specific Integrated Circuit
DSP : Digital Signal Processing
MAC : Multiply and Accumulate
PVT : Process, Voltage and Temperature

TÜM DİJİTAL FAZ KİLİTLEMELİ DÖNGÜLER İÇİN YÜKSEK ÇÖZÜNÜRLÜKLÜ ZAMANDAN DİJİTALE DÖNÜŞTÜRÜCÜ TASARIMI

ÖZET

Tamer Eren

Elektrik-Elektronik Mühendisliği ve Siber Sistemler, Yüksek Lisans

Tez Danışmanı: Doç. Dr. Hakan Doğan

Eş Danışman: Yrd. Doç. Dr. Mustafa Aktan

Haziran, 2021

Faz kilitli döngüler (çevrimler), sadece iletişim devreleri için değil, biyomedikal ve bilgisayar bilimleri gibi diğer alanlarda da kullanılan en önemli modüllerden biridir. Analog, Dijital ve Yazılım tabanlı gibi birçok faz kilitli döngü türü mevcuttur ve bu türlerin birbirlerine göre avantaj ve dezavantajları vardır. Tüm Dijital faz kilitli döngüler, programlanabilirlik ve maliyet verimliliği gibi onları diğerlerinden ayıran birçok önemli özelliğe sahiptir. Topolojiden bağımsız olarak, tüm FKÇ' ler, frekansı giriş sinyalleri arasındaki faz veya zaman farkıyla orantılı olan bir çıkış sinyali sentezlemektedir. Fazlar arası uyum sağlandığında FKÇ "kilitli duruma" girer. Başka bir deyişle, çıkış sinyalinin frekansı giriş sinyali ile aynı olur. Faz kilitleme işleminin ilk adımı, Referans ve Geri Besleme sinyalleri olarak bilinen gelen sinyaller arasındaki zaman mesafesini ölçmektir. Farklı FKÇ türleri, faz farkını ölçmek için farklı alt bloklar kullanır. Dijital alanın avantajlarından kapsamlı bir şekilde yararlanmak için Tüm Dijital Faz Kilitli Döngüler, gelen sinyallerin fazlarını zamana dönüştürür ve bilinen referans açısından varış süreleri arasındaki farkı hesaplar. Bu tezde, 180nm XFAB teknolojisinde 22.18 ps çözünürlüğe sahip hibrit bir zamandan dijitale dönüştürücü tasarlanmıştır. Genel çalışma prensibi, ince ve kaba ölçüm olarak iki kısma ayrılmıştır. Daha sonra Verilog 'da ilk önce üst modül doğrulanmış ve ardından davranışsal Verilog kodları, RC sentez aracı ile "kapı düzeyi" kodlara dönüştürülmüştür. Model Sim'de öncü sonuçlar alındıktan sonra, prototipin şematik seviyesi, önceden tasarlanmış bir Standart Hücre kütüphanesi ile Cadence Virtuoso yazılımında sentezlenmiştir. Hata ölçümü sırasında 1,8 V besleme gerilimi kullanılarak, ortalama akım tüketimi 3.9 mA olarak elde edilmiştir. Fonksiyonel ve periyodik testlerden sonra, önerilen dönüştürücü, ±%10 besleme gerilimi değişimi ile köşe simülasyonlarında test edilmiştir. Ayrıca -200 ^{o}C 'den 85 ^{o}C 'ye kadar farklı sıcaklıklar için aynı testler tekrar edilmiştir. Tüm bu simülasyonlar başarıyla tamamlandığında, önerilen TDC'nin serimi 0.057 mm^2 alan kapsayacak şekilde tasarlanmış ve sonuç Mentor Calibre ile doğrulanmıştır. Son adım olarak, parazitlerin etkilerini gözlemlemek için serim-sonrası parazitik ekstraksiyon simülasyonu koşturulmuştur.

Anahtar sözcükler: TDC, ADPLL, Verilog.

A HIGH-RESOLUTION TIME TO DIGITAL CONVERTER DESIGN FOR ALL DIGITAL PHASE-LOCKED LOOPS

ABSTRACT

Tamer Eren

MSc in Electrical, Electronics Engineering and Cyber Systems

Advisor: Assoc. Prof. Dr. Hakan Doğan

Co-Advisor: Assist. Prof. Dr. Mustafa Aktan

June, 2021

Phase-locked loops are one of the most significant modules that are used not only for communication circuits but also in other fields like biomedical and computer sciences. There are many types of PLLs such as Analog, Digital, and Software-based ones. However, they have advantages and disadvantages among each other, and All-Digital PLLs have many significant features like programmability and cost efficiency that make them stand out from the rest. Independent from the topology, all PLLs synthesize an output signal whose frequency is proportional to the phase or time difference between input signals. When the alignment between phases is achieved, PLL enters the "locked state". In other words, the frequency of the output signal becomes the same as the input signal. The first step of the phase-locking process is measuring the time distance between incoming signals which are known as Reference and Feedback signals. Different PLL types employ different subblocks to measure phase difference. Due to taking advantages of the digital domain extensively, All-Digital Phase-Locked Loops converts phases of the incoming signals to time and computes the difference between arrival times in terms of known reference. In this thesis, a hybrid time to digital converter with 22.18 ps resolution was designed in 180 nm XFAB technology. The overall working principle was divided into two parts as fine and coarse measurement. Then the top module was verified in Verilog first, and subsequently, behavioral Verilog codes were transformed to gate level ones by RC synthesis. After taking preliminary results in ModelSim, the schematic level of the prototype was synthesized in Cadence Virtuoso software with a pre-designed Standard Cell library. The average current consumption during the error measurement was obtained as 3.9 mA from a 1.8 V supply. After functional and periodic tests, the proposed TDC was tested across corners with ±10% supply voltage variation. Moreover, the same tests were performed for different temperatures from -200 ^{o}C to 85 ^{o}C degrees. When all tests were completed successfully, the layout of the proposed TDC was done in a 0.057 mm^2 area and verified with Mentor Calibre. As the last step, parasitic extraction was performed from layout to observe the effects of parasitics in post-layout simulations.

Keywords: TDC, ADPLL, Verilog.

CHAPTER 1

1. INTRODUCTION

Phase-locked loops are one of the most significant modules that are employed in communication circuits as frequency synthesizers. They have many advantages in terms of programmability and cost among crystal oscillators.

Their working principle is based on measuring the phase difference between incoming signals and generating a new frequency whose frequency is proportional to this phase difference [1].

There are many different types of PLLs in literature, however, in this study, a Time-to-Digital converter was designed and proposed for All-Digital PLL.

In the digital domain, instead of utilizing phases of the incoming signals, their arrival times were processed to obtain time difference. TDCs catch these signals and compare their difference with a known reference to compute “phase error” at the end.

There are many methods in the literature for this evaluation process, which are mentioned in Chapter 2. However, the proposed method employs fine and coarse measurement techniques to get a 14-Bit phase error at the output.

The overall structure was built in Verilog first, then the behavioral Verilog codes were transformed to gate level in Cadence Virtuoso by RC synthesis tool. Standard cells that are prepared with 180 nm XFAB CMOS technology are employed for this transformation. Details about the working principle and the design architecture were shared in Chapter 3 and all the codes were given in Appendices. The schematic level of the proposed TDC is tested in different scenarios to investigate the functionality of the system. After all functional and periodic tests were completed successfully, the Place & Route process was initiated and the proposed layout was verified with DRC and LVS tests of Mentor Calibre. All the layouts, simulation results, and the PVT analyses were presented in Chapter 4. To

finalize the simulations, parasitic extraction was performed, and design was tested with parasitics to get the most realistic results. In addition to the individual testing, the proposed TDC was simulated inside a fully functional ADPLL to be sure about the functionality.

As a result, 22.18 ps resolution is achieved in typical corners with a 1.8V supply at room temperature. Moreover, the layout of the design is completed in a 0.057 mm^2 area.

CHAPTER 2

2. THEORETICAL PART

2.1. Phase-Locked Loop Systems

A phase-locked loop (PLL) is a feedback control system that synthesizes a feedback signal with a certain phase to track the phase of a reference. In other words, PLL synchronizes a reference input signal to an output signal in terms of frequency and phase [1].

Phase-locked loops have various types in literature but the main principles behind them are the same. The first step is measuring the time difference between the incoming phase and the feedback phase, and creating an error signal. However, this error signal should be proportional to the amount of phase difference. The second step is making adjustments by changing a control signal with a charge pump and a filter in front of it. The final step is recovering the phase difference between signals by changing the VCO frequency [2].

PLL systems have various working states and ranges which can be listed as;

Locked State

When the phases of the reference and the feedback clocks aligned, which means the phase error between them is “0”, PLL enters into a locked state. In this state, phase and frequency error fluctuations should be very small.

Hold-in Range

This range represents the largest frequency deviations that PLL ensures maintaining the locked state. The loop guarantees to re-achieve its locked position after tracking the new frequency.

Pull-in Range

The Pull-in range states the locking interval of the PLL with an arbitrary initial phase and frequency. The locking process can be long but eventually, PLL frequency becomes stable after tuning of VCO.

Lock-in Range

When the PLL is initially locked, this range covers the frequencies that the system eventually locks again even if there are abrupt changes. This synchronization process can take a long time due to cycle slipping [3].

Phase-locked loops are generally utilized in radios, telecommunication, computers, and other microelectronic applications. The first idea of the PLL comes around the 1920s while trying to achieve resonance between two oscillators.

In 1919, William Henry Eccles emphasized that if two distinct electronic oscillators are coupled to the same resonant circuit, they will eventually oscillate at the same frequency if they are originally tuned to oscillate at close frequencies. However, in 1923, Edward Victor Appleton developed a theory that explains the automatic synchronization between different oscillators [4].

In 1925, the automatic synchronization theory was realized by Professor David Robertson who employs an electromechanical synchronizer to regulate the striking of the Great George's bell. It compares the oscillation of the bell and the feedback signal which is coming from Greenwich Observatory.

Receivers in the analog televisions utilized PLLs, which provide locking to broadcast frequency, for synchronization of the horizontal and vertical pulses, until the late 1930s [5].

Phase-locked loop systems on a microchip were introduced by Signetics in 1969 [6]. After that, the area and power requirements of the PLLs were improved to get a higher frequency range and compact solutions. Today, there are PLLs with areas in the order of only hundreds of μm^2 used for industrial purposes.

2.1.1. Performance parameters of PLL

There are different parameters that determine the working range and the quality of the PLL systems. They are fundamental indicators of performance and can be traded according to the application.

• The most significant parameter of PLL is locking and capturing ranges, which can be also considered as the frequency band of PLL.

• Sensitivity is also another parameter that shows the quality of PLL. This property is directly related to the VCO block, and it shows the rate of change of created frequency with respect to unit increment in the error signal. The resolution which shows the closest distinguishable phase difference is also another important parameter for PLL and it determines unachievable phase differences, or in other terms offset error in locking condition.

• Locking time and transient response of the PLL also affect the function and the quality.

• Power consumption, the amplitude of the output, and area are some of the common considerations for all PLLs as well.

• Jitter and noise performance is also another significant parameter to obtain a clean frequency spectrum at the output [7].

To describe the working principle of the phase-locked loop systems, some properties should be explained extensively. One of the main properties that indicate the price and efficiency of the PLL is the level of sensitivity. The sensitivity or the minimum frequency steps of the VCO is important for fine-tuning the PLL. When the error output of the phase detector varies slightly, the frequency of the VCO should not change by a large amount. In addition to that, the frequency band of the VCO directly indicates the working range of the PLL, in other words, capturing range of the system.

Moreover, the resolution can be described as the closest measurable distance between rising edges of the reference and feedback clocks in the locked state. Phase detectors or TDC architectures are the main determinants of resolution in PLL systems [8]. Furthermore, phase error in the “locked state”, in other words, the time difference between the phases of the input clocks is called static offset error which is inevitable. Even for very low operating frequencies, there will be some errors due to the non-zero

delay between the phases of clocks or delay lines. PLLs cannot resolve these differences because they are smaller than the resolution of the system.

In ideal circumstances, the static phase offset should be zero, which means, in lock condition reference and the feedback clocks have to be aligned. However, adjusting and lowering this static offset, which means increasing the resolution can solve jitter issues, and phase noise is the most common type of jitter observed in PLLs [9]. Jitter is almost inevitable for PLL systems and it is originated from the oscillators. The tracking jitter should be as low as possible to increase the performance of the PLL system. Phase noise can be minimized by the careful design of the sub-blocks of the PLL as well as by optimizing the overall top-level PLL system. Furthermore, sudden changes in the supply voltages, ground nets, or substrate noise affects jitter performance. Consequently, PLLs with higher noise rejection have better performance [10]. An injection or self-injection oscillator can be applied to obtain better phase noise in the VCO block of PLL [11].

2.1.2. Usage of PLLs

Phase-Locked Loops are generally used in processors, FPGAs, and radios for generating the system clock or the RF frequency. The main fields that use PLL are unsurprisingly electronics and communication because compatible demodulation of incoming signals with an internal signal is a fundamental requirement of these fields. Synchronization of the bits in digital communication is also another purpose of employing Phase-Locked Loops.

By employing PLLs, new frequencies can be synthesized which are multiple or the same with a reference frequency in the microchips. These new frequencies should meet the stability constraints of the reference clocks. Generating new frequencies with PLL in higher bands is also much cheaper than using high-frequency crystal oscillator solutions.

There are some other applications of PLLs such as frequency demodulation. If the output of the phase-locked loop is locking to a frequency modulated signal, the voltage-controlled oscillator should adjust itself to the instantaneous frequency of the input signal. VCO of the communication system controls its output via error signal and PLL should cover all the ranges of VCO as linear as possible [12].

The same procedure also applies to phase modulation as well. However, this time, the phase of the system is much more important and PLL should cover this phase range for successful demodulation [13].

In digital communication, instead of using an analog signal directly, digitally generated bits and symbols should be transmitted via carriers. Computers, routers, or any kind of transmitter-receiver pair uses PLL to catch and track carrier frequencies of these binary data which is shifted between two or more frequencies.

Amplitude demodulation can be another perspective for the usage of PLLs [14]. AM signal's carrier can be recovered in terms of phase and frequency by PLLs and generally, the phase of the recovered signal is obtained with a 90^{o} degree phase shift. PLL-based amplitude modulation detector tends to have excellent selectivity and enhanced noise immunity due to the working range of the PLLs in specific bands around carrier frequencies that are also close to the output of VCO [15]. Phase-Locked Loops are also employed in a modulation part, where specific frequencies should be synthesized.

Other than communication systems, there are various applications that need a PLL for several purposes. For instance, microprocessors and computers need an internal system clock to process the data. Generally, crystal oscillators were employed to obtain the main frequency due to the high precision requirement. However, other frequencies, which are multiples of the main one, can be obtained via PLLs. Moreover, the multiplication constant can be quite large to obtain operating frequencies in the gigahertz band where the reference crystal is in the megahertz range [16].

Clock and data recovery is another application for the PLL systems. Basically, CDR extracts the received data stream which is coming from the receiver. In these types of systems, distortion can lead to loss of clock information, and PLL recovers or regenerate proper clocks [17]. In this case, the transition of the data should meet the frequency range of the PLL to be able to create or track frequencies.

Furthermore, one of the main implementations of the PLL is preventing or minimizing the effects of skewing in digital circuits. Skewing can be explained as different arrival times of the same clock to the input of different gates. If the delay causes a phase shift, this can lead to serious synchronization and timing problems in the overall system. The deskewing function of the PLL is employed to align these skewed clocks to the original input and match the phases [18]. For this kind of application, the delay-locked loop is much more applicable rather than conventional phase-locked loops. DLL creates a delay line and compares the phase of the input and reference signals. After filtering of mismatch

between these signals, the result is used in the VCO and the phase of the control signal is adjusted.

In addition to the fields represented above, PLLs are employed for the synchronization of video signals [19], boosting the microcontroller's operation clocks [20]. Also, in Biomedical, they are utilized in surface-tip relations of Atomic Microscopy [21], reduction of electromagnetic interference in ECG systems [22], and clock generation for implantable biomedical devices [23].

2.1.3. Types of Phase-Locked Loops

Almost every single application requires different properties and specs from phase-locked loops and these different requirements can be met with various types of PLLs. Analog applications require relatively low phase-noise phase-locked loops. For instance, radio receivers and transmitters could use Analog PLL systems. Moreover, the combination of the analog and digital components (blocks) creates a digital phase-locked loop (DPLL), and if all modules in the PLL are synthesized digitally, it becomes an all-digital phase-locked loop (ADPLL). However, for software applications that are not designed physically, there are software phase-locked loop (SPLL) systems as well [24]. In **Figure 2.1**, differences between blocks of Analog and Digital PLL can be examined.

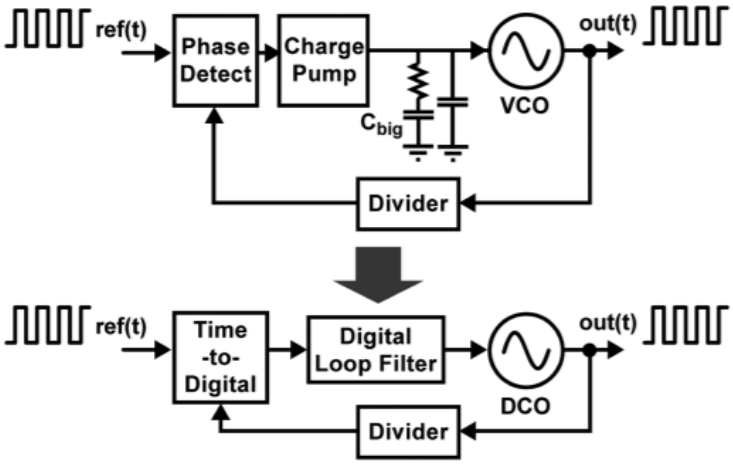

Figure 2.1: Transition from Analog PLL to Digital PLL [25].

Analog or Linear PLL (APLL)

Analog phase-locked loops employ phase detectors which are designed as an analog multiplier to detect incoming phases. Basically, it generates a product of two incoming signals to extract their phase correlations. The output of the phase detector acts as an error

signal and directly feeds into a filter that smoothes the phase difference. At the output of the filter, a voltage-controlled oscillator generates an oscillation frequency as a function of the incoming filtered error value. The overall system uses the VCO output to generate feedback to reduce the difference between the two phases.

Digital PLL (DPLL)

Digital phase-locked loops combine the function of analog PLLs with digital blocks. Instead of using an analog phase detector, flipflop and XOR-based digital blocks measure the phase difference between the incoming phases. Furthermore, a digital filter and a digitally controlled oscillator can be utilized in digital PLL.

All digital PLL (ADPLL)

Without using any analog modules or submodules, every single function in the analog PLLs is mimicked via digitally synthesized modules. Time to digital converters are used rather than an analog phase detector, and filtering can be achieved digitally. Moreover, the result of the filter is used as a control input for the fine and coarse tuning of the digitally controlled oscillator. In the feedback loop, a frequency divider with a sigma-delta modulator can be utilized for generating the feedback signal.

Software PLL (SPLL)

As an alternative to physical hardware, all the functions of phase-locked loops can be implemented via software. Software PLLs can be standalone modules as well, but they are also a good practicing method to solve functioning issues before synthesizing the circuit.

2.1.3.1. Analog PLL blocks

The function of the phase-locked loops is almost the same for every type of PLLs. On the other hand, the types of the blocks can be changed, and in **Figure 2.2**, the most common configuration of the Analog PLL blocks is shown.

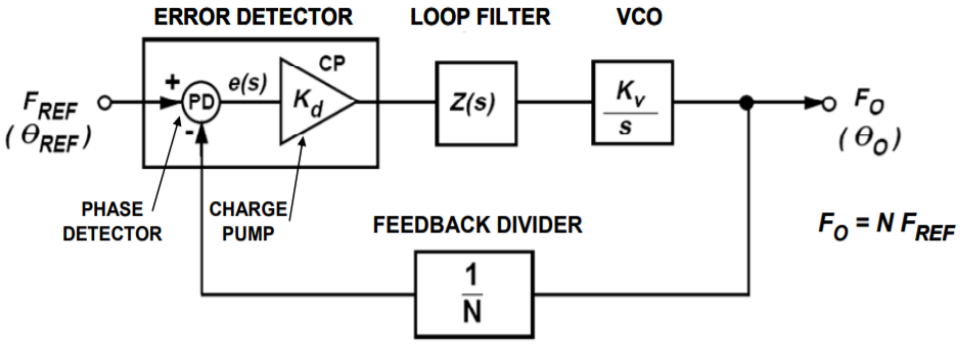

Figure 2.2: Blocks of Analog PLL [26].

Phase detector or time to digital converter measures the phase or time difference between incoming signals to generate an error signal that is proportional to the phase difference. After low pass filtering of this error, voltage or digitally controlled oscillator generates a periodic clock. The frequency of this signal is controlled by the error signal, in other words, the output of the oscillator is also proportional to the phase difference between two signals. Furthermore, a feedback divider is implemented to facilitate the evaluation process in the phase detector which will be mentioned later.

Phase Detectors

The phase detector takes in two signals at the input side and generates an error signal which demonstrates the difference between the 2 phases. These phases are known as reference input and feedback from the voltage-controlled oscillator. In each measurement, the output of the detector feeds a low-pass filter to eventually control the output frequency of VCO. The sensitivity of the phase detector is the most significant property for this module and PLL loops continue until the phase error becomes “0” [27]. Phase detectors in analog PLLs are designed at the transistor level with a multiplexer idea. In **Figure 2.3**, an example for a transistor-level analog phase detector is demonstrated.

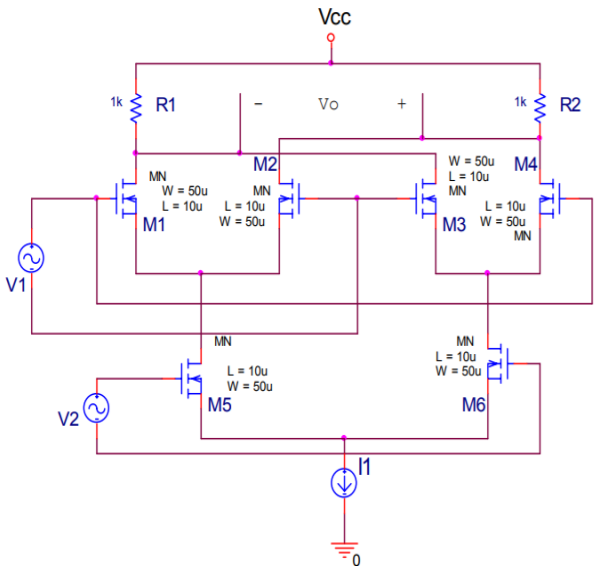

Figure 2.3: Analog based Phase Detector [28].

Frequencies of the input signals were multiplied and compared to get two different frequencies in output which represents phase differences of incoming signals.

A conventional solution to ensure stability in phase error signal is using a charge pump, which is fed by the output of the phase detector. It regulates voltages which will be used as an input of the low-pass filter, using charge pumped into a capacitive-energy storage element [29]. Charge pumps guarantee high-efficiency solutions for low output current applications. Also, they provide constant and stable output with varying error input.

Analog Filter

Almost all types of PLLs employ a loop filter that shows low-pass characteristics for regulating the error signal from the PD.

The most significant function of this loop filter is adjusting the loop dynamics, which are bandwidth, gain, and stability. Also, the order of the filter is important and directly affects the performance of the PLL. The schematic of a 3rd order PLL filter commonly used in PLLs is presented in **Figure 2.4**. The bandwidth of the PLL is determined by the filter and it also regulates the lock range and lock speed of the overall loop. Moreover, the filter ensures the stability of the systems when it is disturbed due to sudden interferences and disruptions at reference and feedback clocks.

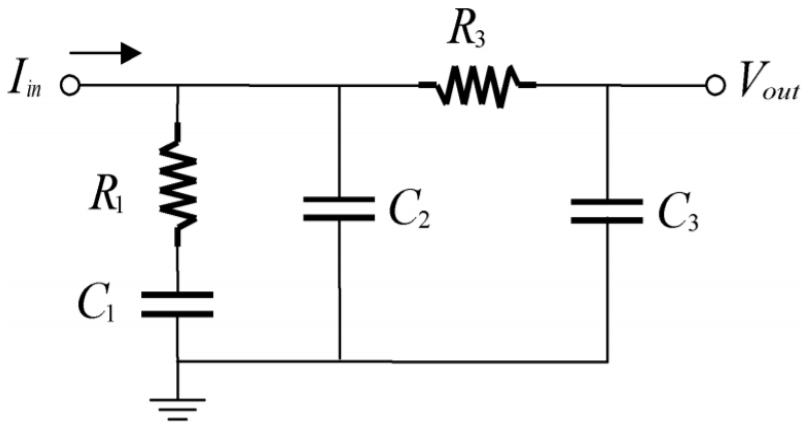

Figure 2.4: Third Order Analog Loop Filter[30].

The second property of the filter is adjusting the amplitude of the incoming error signal. A filter can be utilized to increase the amplitude as well as to attenuate it. Gain and phase margins of the PLL are the most important design parameters for this regulation [31]. A low pass filter is also employed to limit the amount of ripple on the VCO control voltage. Also, filtering is significant to ensure the lock condition and reducing the number of spurs at the output. Phase noise is another important parameter for filter design that can affect the design parameters of the filter.

Voltage Controlled Oscillator

The Voltage Controlled Oscillator is the main component of the PLL and is controlled by the loop to generate the desired frequency. The first and the most significant property of this block is the frequency range. Voltage-controlled oscillators adjust their outputs via an incoming control signal. These adjustments and the generation of the oscillation frequency can be realized in various ways. One of the most common methods is taking advantage of the resonance between an inductor and varactor that changes its capacitance with the change in control voltage. This type of VCO is called the LC oscillator and **Figure 2.5** shows the schematic for an NMOS-Only LC oscillator. Varactors can be obtained via a reverse-biased diode which is controlled by the control voltage and they have wide range capacitance ratios [32]. In addition to them, there are inverter-delay-based ring oscillators as well [33].

Generally, the frequency of oscillation should be stable as possible regardless of the type of the VCO.

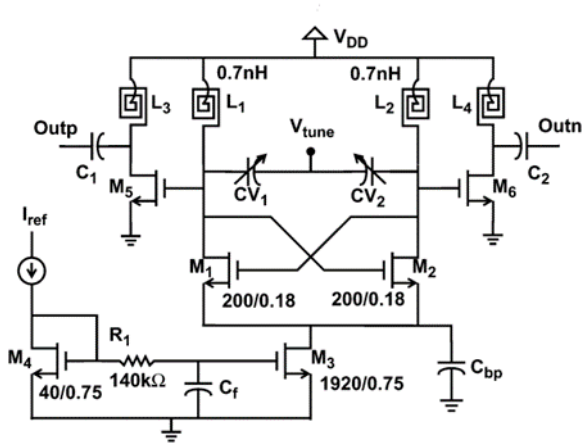

Figure 2.5: Voltage Controlled Oscillator Schematic [34].

After measuring the phase difference in the phase detector, the obtained error signal indicates any required increment or decrement in the oscillation frequency of the VCO. For instance, if the output frequency of the VCO signal is lower than the desired value, which means the phase of the VCO falls behind the phase of the reference, the error will affect control voltage positively to increase the VCO frequency and vice-versa e.g., if the phase of the reference is behind the feedback clock, then the frequency of the VCO is lowered.

Feedback Divider

The adjustable frequency divider is another common block that is used in the feedback line of the PLLs. They use the output of the VCO to generate a new frequency which is a rational multiple of the newly synthesized clock. Thanks to the divider in the loop, the previously generated clock can be varied into many frequencies which is not possible by using the VCO only.

The range of division ratio is the most significant parameter in the divider design. However, rational multiples of the main frequency can be achieved easily by using registers such as given in **Figure 2.6**.

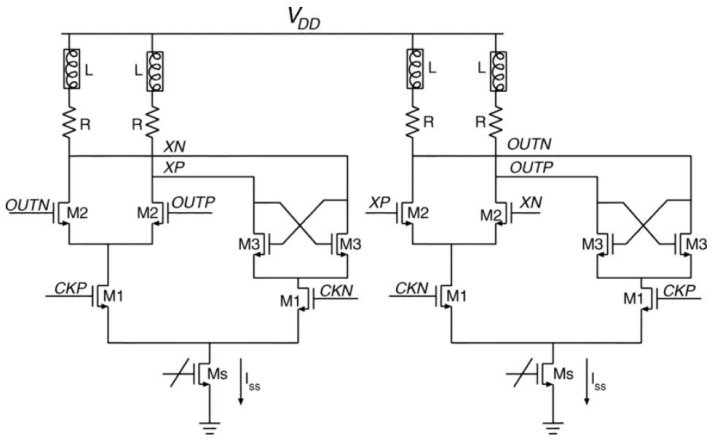

Figure 2.6: D flip-flop based Frequency Divider [35].

On the other hand, dividing the feedback clock with fractional numbers is more cumbersome than the normal division. These kinds of applications require multi-modulus divider blocks to determine the division ratio of the signal. Sigma delta modulators with various orders are generally used for fractional division. The main principle behind them is to randomly vary the division ratio to achieve an average divide ratio [36].

Furthermore, working in low frequencies eases the speed requirements significantly, hence some PLLs utilize a high-speed pre-scaler to scale the high-frequency VCO output to more manageable lower frequencies.

2.1.3.2. Digital and All-Digital PLL blocks

Even though All-Digital phase-locked loop systems have the same function as Analog PLLs, there are significant differences in terms of performance and building blocks between them. First of all, All-Digital PLLs tend to have a smaller locking time than analog devices at the same frequency band [37]. Moreover, All-Digital phase lock loops maintain their lock conditions even for sudden changes in the reference clock in terms of phase and frequency. In other words, losing the locking state is much harder than the analog PLL systems. Even they can reject noise and jitter more successfully than analog PLLs, their size is bigger because of the additional adder and divider blocks. However, the integrity of the design highly depends on the process, and the sizes of the filters are the main indicators for the size of the overall architecture. On the other hand, in terms of cost and complexity of the design, analog PLLs can be a better solution rather than digital ones. Furthermore, All-Digital PLLs can be utilized in high-frequency RF synthesizers with high resolution and fast settling [38].

After the development of DCO, researchers achieved precise frequencies that can be controlled via reference digital words. There besides, designing the smaller and faster digital gates facilitated the transition from the analog to the digital domain. Eventually, in the late 1980s, the All-Digital PLL idea was started to grow, and in the 2010s field-programmable array-based PLL was proposed [39], [40].

Phase Detectors – TDC

Before using "All-Digital PLLs", various types of digital modules are utilized as a detection of the phase in the "Digital PLLs". The easiest and most famous one is the simple XOR gate. When the signals have different levels, output automatically becomes logic 1 to show the unmatched regions. There are 2 main issues in XOR implementation. The first one is a lack of sensitivity at the edges of the signals and the second one is the inefficient measurement of difference. To calculate or understand the phase difference exactly, time at the logic 1 state of the output should be measured with a stable reference.

Also, J-K or D flip-flops can be utilized like in **Figure 2.7** to get an error signal that changes due to the phase error between reference and feedback clocks. However, again the main problem is dividing the overall error into fine and coarse parts which should be considered distinctly.

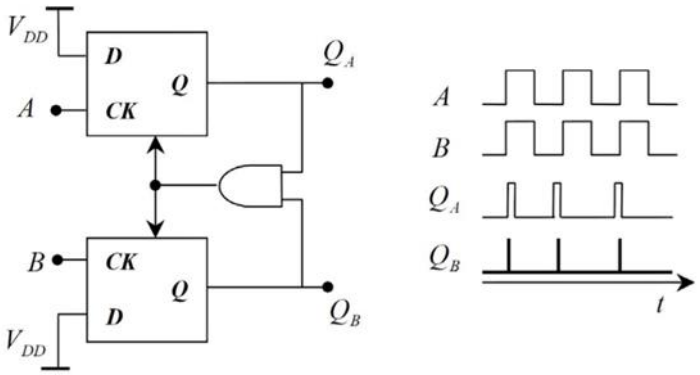

Figure 2.7: Digital Phase Detector [41].

Bang-bang architectures are another common type of phase detector that can be used in all-digital PLLs. Basically, it operates with D flip-flops for the detection of phase in "up" and "down" conditions [42].

When the transition from Digital PLL to All-Digital PLL is completed, phase detectors were transformed to the Time-to-digital converters which can hold the incoming phases

as a time substance and divide them by well-known coefficient. Design steps and all examples about TDCs will be presented in the next chapters.

Digital loop filter

Without using any passive elements like resistors or capacitors, basic programmable integrators and delay elements are utilized for low pass filtering [43]. Functionality and programmability of the filter are designed by synthesizing it from VHDL or Verilog codes. **Figure 2.8** shows the block diagram of a digital low pass filter that is designed in this project. Regulation of the bandwidth and the gain is also much easier in digital filters and also the locking speed of the PLL system becomes adjustable via this approach.

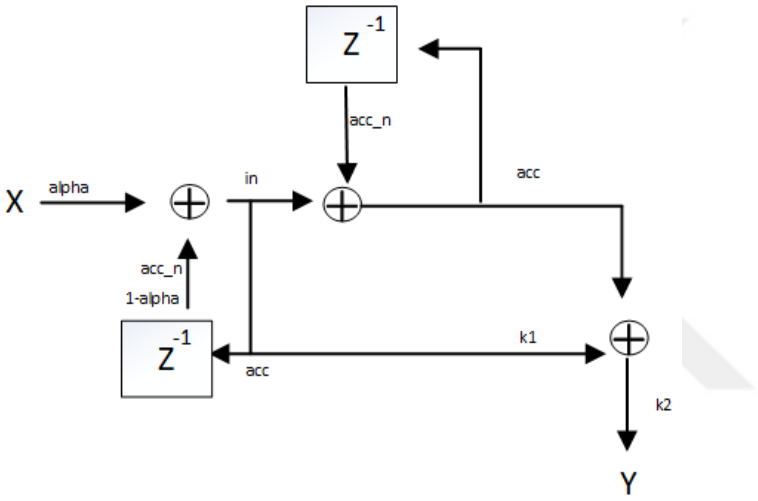

Figure 2.8: Block Diagram of Digital Loop Filter.

Digitally Controlled Oscillators

Instead of using a control voltage to regulate oscillation frequency, digitally controlled oscillators utilize incoming error bits to control oscillation. Simply, digitally controlled oscillators combine the function of VCO with the working principle of a DAC [44]. There are various types of DCOs that are designed to use be used in different frequency ranges. MOS Varactors and capacitor arrays are used to control the frequency of the DCO. Nevertheless, obtaining a stable frequency, and maintaining that specific point is the most significant specification for the DCO. A Digital feedback divider is employed after the DCO to divide the clock for comparison with the reference clock. Their functions and working principles are almost the same as the analog ones.

2.2. Time-to-Digital Converters

Time-to-digital converters are employed as phase detectors for all-digital phase-locked loop systems. Before phase-locked loop applications, TDCs have been utilized for more than 20 years in the applications of nuclear physics and biomedical where measurement of precise time-interval is required [45]. The first step of the time to digital converter is catching the rising or falling edges of 2 clocks and producing an error that will be proportional to the "time" difference between edges of the inputs. The most common field that embeds TDCs into the center of their system is communication electronics. However, other fields such as logic analyzers and digital scopes are also important applications of TDCs. Furthermore, almost every single time-of-flight measurement requires specific TDCs for the calculation of time intervals.

Analog circuits should be highly linear and precise to process the data which is placed into the envelope (amplitude) of the signals. Conversion and digitization of this data into the time domain facilitates signal processing and also eases the design of the overall systems. For this kind of application time-to digital or digital-to-time converters can be utilized. Moreover, TDCs can be used as a subsidiary element of ADCs for digitization purposes. The first example of a TDC was developed in the year 1942 by Bruno Rossi for the measurement of sub-atomic particle lifetimes [46]. It was designed as a time-to-amplitude converter, which charges a capacitor during the measurement of the two distinct events. On the other hand, until the end of the 1990s, analog signal processing in the time domain with TDCs has not become popular due to the micro-scale-based transistor technologies [47].

In terms of area, speed, and power, digital circuits benefit from the edge on improvements of transistor sizes, and in the deep sub-micrometer domain, analog and digital circuits started to use the time domain measurements for signal processing. In the first examples of TDCs, the resolution of the time interval between reference and feedback measurements has required nanosecond levels but recent developments demonstrate that synchronization of the clocks can be achieved in femtosecond levels. As a result, transmitters and receivers employ all-digital phase-locked loops (ADPLLs) which digitize the phase shift between clocks by TDCs.

2.2.1. Performance parameters of Time-to-Digital conversion

Although all TDCs perform the same function, some performance parameters vary depending on the application. In other words, time to digital converters digitize or quantize the time difference between inputs, but the required speed, area, and bandwidth of the operation can change. Some of the parameters should be explained in detail to understand the working principle and developing process of the TDC in this study. Principally, the performance parameters of TDCs are close to ADCs but they have some unique characteristics that are due to time conversion.

2.2.1.1. Resolution

The resolution of a TDC is the most fundamental and significant parameter that describes the smallest distinguishable time difference value that the converter can achieve. Recent CMOS processes detect time differences in femtosecond levels. Even though it is negligible in state-of-the-art solutions, finite resolution causes quantization noise, which can be considered as the static offset. If the system employs a ring oscillator to measure the time difference, the delay between each element indicates the resolution. Essentially, as with the LSB of an ADC, the resolution is a step width in the quantization characteristics of a TDC, which can also be explained as the range of continuous-time inputs that are transformed to the same digital word [45]. Actually, the resolution is an intangible term, but it can be examined in **Figure 2.9** conceptually.

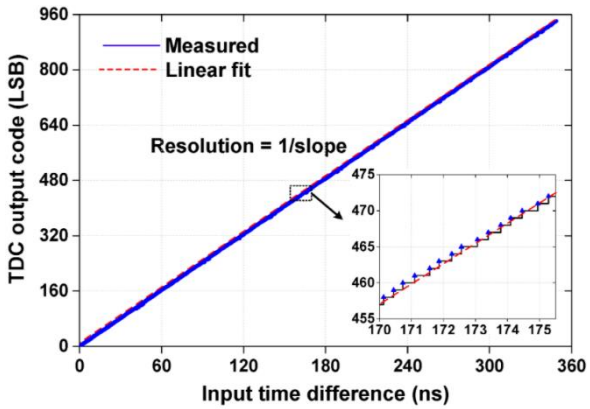

Figure 2.9: Linearity and Resolution graph of TDC [48].

2.2.1.2. Output bits

The number of the output bits (NoB) determines the maximum time difference that the TDC can resolve. The output of the TDC goes through a filter and indirectly regulates the oscillation of the VCO. In other words, the number of output bits controls the detectable

range of the PLL. Using an adequate number of bits is important to determine the locking range of the PLL as well as power consumptions [49].

Essentially, the dynamic range can also be explained as the maximum time difference that TDC can measure. Above that level, TDC gives the same results for all differences, in other words, it enters the saturation region. In some of the applications, the dynamic range determines the maximum measurable time difference. For instance, in LiDar implementations, the detectable longest distance depends on the dynamic range of the system. Dynamic range can be increased by using more bits in the error signal. However, area and power limitations prevent the usage of long digital words in the output. Moreover, filter or charge pump design is directly related to the length of output error. In other words, making arbitrary changes may not be possible when all the design aspects are considered. The correct way to determine the dynamic range of the TDC depends on the application it is designed for. For PLLs, it directly depends on the reference signal and the oscillation frequency of the VCO. On the other hand, in time-of-flight PET, the TDC should cover all the possible annihilation points, which are the source points for gamma emissions in a specific range of detector rings [50].

2.2.1.3. Linearity and non-linearity

Principally, a time-to-digital converter is a subcategory of an analog to digital converter and like all the other data converters, one of the most important properties is the linearity of the operation. For 50 ps resolution, 1 ns phase difference between two clocks should give 20 as a “phase error” output in conformity with linearity property. Similarly, the 2 ns phase difference should give 40. The linearity property of the TDC can be affected by phase noise, device mismatches, and parasitic capacitances. Moreover, the delay between ring oscillator phases can cause nonlinearity. There are various ways to improve the linearity of TDCs and one of them is employing less amount of delay between phases of the ring oscillator [51]. If delays between buffers or inverters are not equal to each other, this phenomenon can cause an unbalanced calculation of the phase error.

The linearity stipulations of a PLL can be categorized as the dynamic performance of a system and DC accuracy [49].

In an all-digital phase-locked loop system, phases of the incoming signals are almost time-invariant at the locked state. In other words, during the locked state, the input of the TDC does not change in time.

On the other hand, because of the nonlinear characteristics of data transformation, harmonic distortions may occur as in any converter. These distortions are observed as spurious tones in the output spectrum, and they can even be obtained in the locked state. Besides, not only TDCs but also the overall PLL systems can suffer from these nonlinearities. Due to these reasons, possible nonlinearities should be designated before any implementation. Unfortunately, TDC modules should have finite resolutions in the picosecond levels, and this behavior results in extra quantization noise which can affect the output spectrum of the PLL negatively [52]. However, increasing the resolution still important because the effects of quantization noise become negligible if it is smaller than the phase noise of DCO.

Any type of nonlinearity can be detected from the monotonicity and integral nonlinearity (INL) graphs [49] as is shown in **Figure 2.10**.

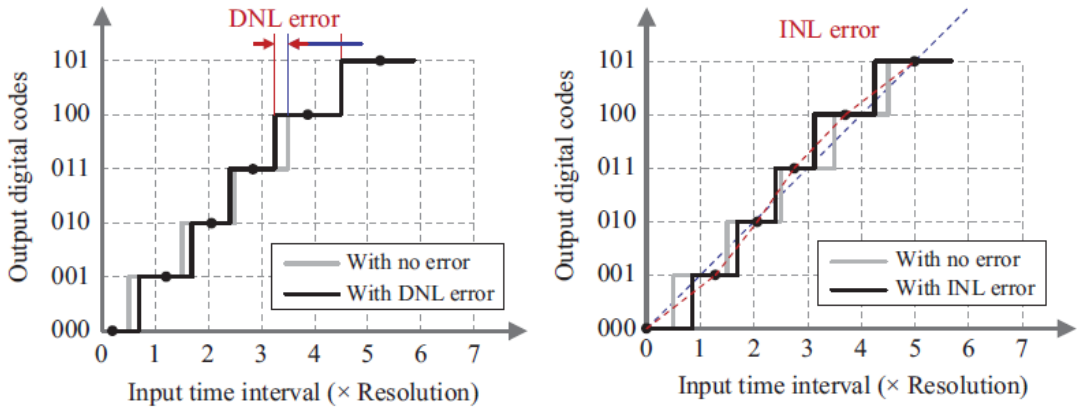

Figure 2.10: a) DNL of TDC, **b)** INL of TDC [49].

Integrated Non-Linearity (INL) is the difference between the expected and measured output values for a specific input code. Also, there is another important linearity metric for data converters given as Differential Non-Linearity (DNL), and it demonstrates the amount of variation between the two subsequent digital outputs from the ideal step. Principally, INL is the summation of the DNLs for the overall word as is shown in equation **2.1.**

$$INL_n = \sum_{i=0}^{n} DNL_i \qquad \textbf{(2.1)}$$

2.2.1.4. DC accuracy

DC accuracy of a TDC states the worst-case variation of the transfer function from a linear response in terms of gain and offset error.

Transfer function:

The relation between the time difference between incoming clocks, and the output error signal can be presented with a transfer curve of the time-to-digital converter.

Gain error:

The difference between the ideal and actual transfer curves of a TDC in a time scale is known as a gain error. In other words, the maximum time difference of the clocks will be represented with fewer bits, and it will change the slope of the transfer curve.

Offset error:

TDCs should not generate an error signal at the output without any input clock or 0 phase difference conditions. This problem can lead to LSB shifting in the transfer curve and also affects the frequency of the oscillation in VCO. An example graph for the offset and gain error is presented in **Figure 2.11**.

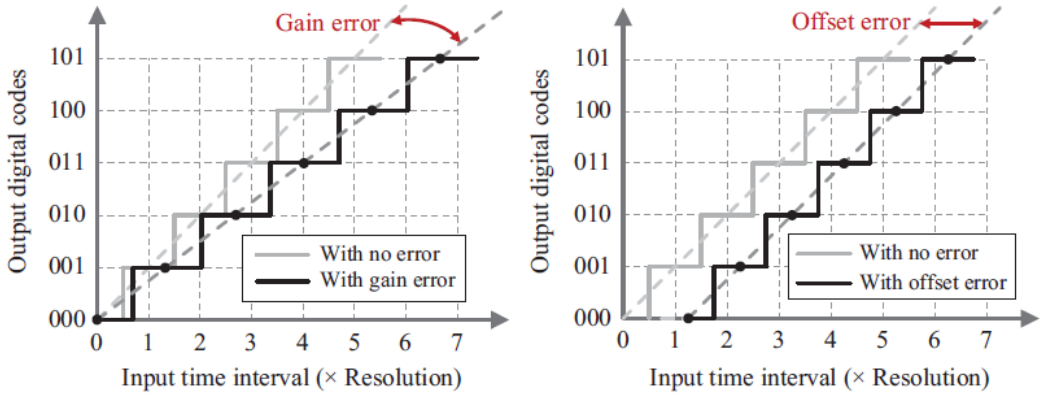

Figure 2.11: a) Gain error graph **b)** Offset error graph of TDC [49].

2.2.1.5. Power and area

Like all the other electronic components, the ultimate requirement for TDCs is achieving the best performance with less power in a smaller area. The development of smaller transistor feature sizes that also minimize the power consumption is the first key to meet optimum solutions. Furthermore, the function of the TDC can be developed with an architecture that minimizes the area of the solution on a chip.

Nonetheless, any delay line-based oscillator that is used as an internal reference will consume a big portion of the power, and there are various design methodologies to reduce the power consumption of these elements [53]. However, if TDC is synthesized via a design synthesis tool, standard cells with low power dissipation should be utilized.

2.2.1.6. Dead time and counting rate

The dead time of a time to digital converter is one of the most significant parameters that show the quality and the performance of the system. It can be explained as the required time to complete digitization of the single time difference. Each application demands different dead intervals to achieve successful digitization. For example, high-speed machine learning and image processing applications require fast samplers to recreate images. Moreover, positron emission tomography (PET) also needs small latency between samples to create an image of a tissue or body. For these implementations, TDCs with small dead time and large counting rates can be employed to increase the quality of the final product. State-of-the-art methods can achieve up to 7.5 ns dead time which is good enough for almost any application [54]. However, if the overall frequency of the system is increased, the dead time of the one-clock-cycle-based designs improves.

On the other hand, finite dead time is inevitable for systems that have a single calculation unit even if the time distance is very small. However, there are many approaches and design techniques to limit the dead time. Employing parallel calculation units in a single TDC architecture is one of the most famous solutions for dead time. The fundamental working principle is when one of the processors starts to measure the time difference, the other one waits for the new signal. In other words, while one of them is working, the other one stays in a hold mode, until a new signal arrives during the measurement process. Some of the interleaved topologies were proposed [55], [56] to reduce dead time and increase digitization rates.

2.2.2. Usage of TDCs

There are so many applications of TDCs which are outside of PLLs as well. Even though all previous examples are related to PLLs and time to digital converters and DTCs are the signature blocks for ADPLLs, TDCs can be utilized in the time interval measurements individually. Also, the phase-shifting process takes advantage of digital-to-time converters which can also be used as a time delay element.

Time to digital converters are utilized not only for communication or RF engineering but also in physics and biomedical devices. Positron Emission Tomography (PET) and Fluorescence Lifetime Imaging (FLIM) are good examples of TDC applications in medicine [45]. They use time of flight measurements, which are also the same as absorption time measurement techniques, to create a detailed image of the tissue. In PET

systems the time difference between two opposing gamma-ray emissions, and the event signals can be measured with TDCs precisely [57].

Coincidence counters also utilize time-to-digital converters as time taggers. Simultaneous detection of subatomic materials within a microsecond level requires high-end counters and they use the time to digital converters to hold and measure the time difference between 2 particles, which are emitted from the same nucleus [58].

These counters have a significant role in quantum physics and biomedical imaging experiments for measuring the correlation of gamma-rays. In a PET scanner, gamma radiation from the destruction of the positron-electron pair was examined via detectors after a substance that can emit positrons is applied to a subject. The location of the subject organ or tissue can be found by counting the time between emission and detection. This time information is used for calculating the exact coordinates of the radio-tracer substance as well. TDC-PET combination given in **Figure 2.12** is employed to digitize gamma-ray pairs' times of flight times after detection [59].

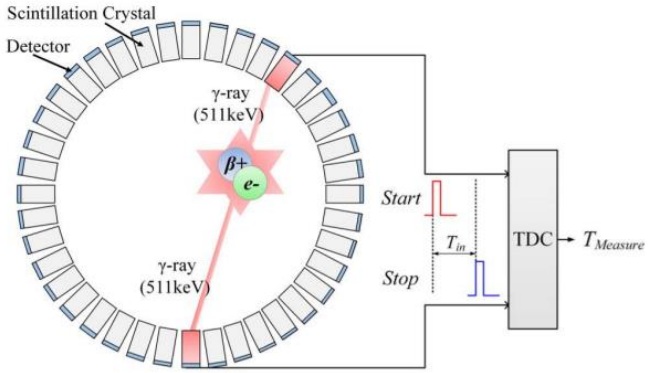

Figure 2.12: Time-to-Digital Converter in PET Systems [45].

Spectrometry is another biomedical application where TDCs are commonly used. Distinguishing a substance that contains different materials can be a good definition for spectrometry. Because of the different masses and charges of ions, they can be classified with respect to their interactions with light. One of the most known spectrometry examples where TDCs are utilized is Time of Flight Mass Spectrometry (TOFMS) [60]. In TOFMS, after ionization of the molecules, they are accelerated until reaching the same kinetic energy and because of different masses, arrival times will vary for each substance. However, when the initial time is known, the difference between the starting point and the arrival time can be measured via TDC.

Time of flight tomography utilizes the same principle behind the TOFMSs, and they also employ TDCs for biomedical imaging. Moreover, fluorescence spectroscopy utilizes time

to digital converters to successfully measure the decay time between light-excited substances. Each time difference pulse represents different molecules [61].

In laser imaging detection and ranging (LiDAR), the most important parameter to recreate an image is the time difference between the emission from the source and the arrival time of the reflected photons. The detection time between these signals is also utilized to measure the distance between target and source. TDC quantizes and digitizes this distance for further signal processing [62]. The detailed working principle of the LiDAR system is presented in **Figure 2.13**.

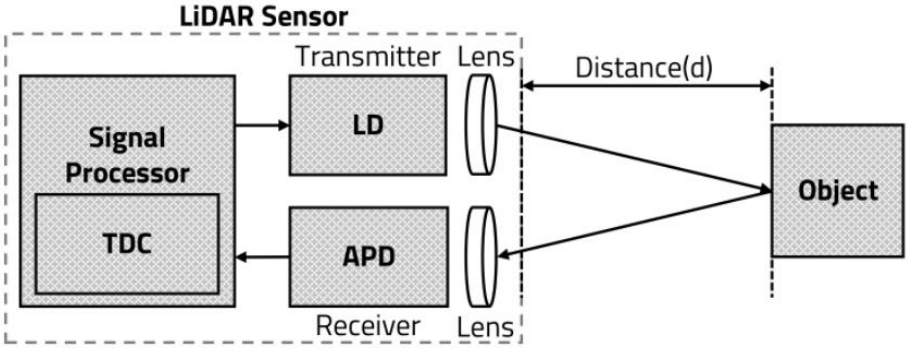

Figure 2.13: TDCs in LiDAR applications [63].

In the RF domain, because of the high frequencies, the required minimum detectable time interval should be smaller than the less sensitive applications. These kinds of applications expect high resolution from TDCs, and their design is more complicated than others.

A couple of picoseconds or even femtosecond resolutions can be utilized for these purposes. Also, the bandwidth of the TDC should be higher in RF applications and this requirement is directly related to the dynamic range of the TDC's output. More bits in the output mean that more space to represent bigger errors in time [64].

Furthermore, a successful TDC should be fast between the calculation of successive time differences. If a new time difference comes during calculations, the overall PLL loop can be broken, and the system gives erroneous results which can lead to misregulation of the oscillation frequency of the VCO. The time digitization operation needs to be as linear as possible to ensure each digital step represents the same time difference. This behavior is extra important in the RF domain because even small amounts of miscalculation of the error can cause bigger problems in the system. Actually, independent of the frequency range, all TDCs should have a wideband working range, high resolution, and fast operation specs between each successive (periodic) time conversion process [65].

Rather than using signal processing, some of the deep learning techniques can be utilized with TDCs. For instance, the performance parameters of TDCs such as nonlinearity can

be modeled and optimized via neural networks and machine learning algorithms in FPGAs [66]. Moreover, Internet of things applications and fast AI programs which are also known as edge inference systems take advantage of TDCs to regulate their time-dependent network plans [67].

2.2.3. Working principle of classical TDCs

Independent from the architecture, the main purpose of the TDCs is to calculate the time difference between incoming signals. In other words, a phase difference between two incoming signals should be converted to digital bits in TDCs. This transformation process relies on ADC functions with small differences. **Figure 2.14** illustrates the well-known working principle of TDCs. The Start signal initiates the counting process and when the stop signals arrive, coarse counting is terminated. Phases of the incoming signals should be recorded first. Then the difference between those recorded points should be measured with a known delay. This known or "reference" interval can be generated via simple delay lines or ring oscillators.

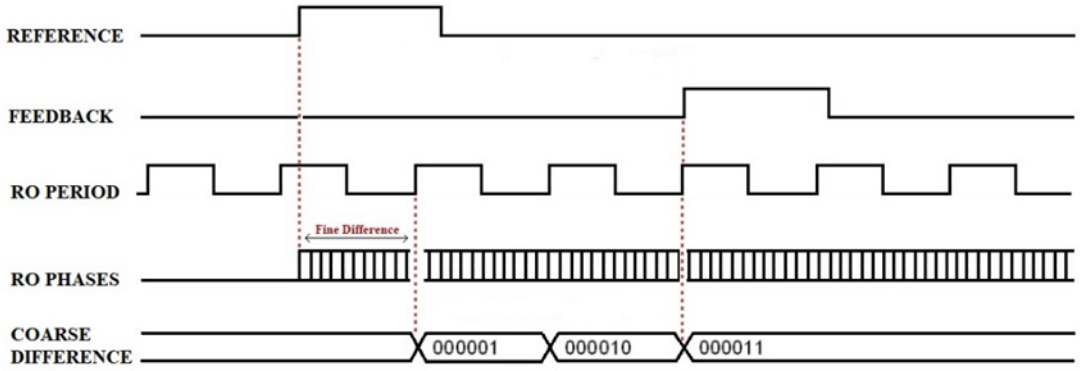

Figure 2.14: Working principle of TDCs.

However, to achieve higher resolutions in state-of-the-art, high-end applications, fine counting can be necessary.

There are common expected parameters from TDCs like high resolution, wide dynamic range, lower power consumption, and low phase noise. On the other hand, these parameters, or trade-offs between them vary among applications.

The output of TDCs is generally calculated as thermometer codes, but there are other ways to obtain the digitized difference. There are various topologies for TDCs that can be used for different implementations in analog and digital domains. Internal structures of these TDCs generally remain the same, which contains delay lines, registers, and

counters. However, the number and type of each element depending on the requirements of the applications.

2.2.4. Time-to-Digital Converters architectures

There are numerous types of TDC architectures that were designed to achieve the required performance and make the trade-off between resolution, area, dead time, and detectable range, in literature. Moreover, power consumption, cost, and conversion speed are the other parameters that should be considered during development. The main types of different TDC architectures are demonstrated below.

2.2.4.1. Counter-based TDC

Counter-based architectures can be considered as a primal version of TDCs, which were generally used before the development of sub-micron CMOS devices. For low-resolution applications, in which a couple of nanoseconds is required for conversion, counter-based TDCs can be employed. The main working principle of the counter-based TDCs depends on a high-speed counter architecture. In each clock cycle result of the output is incremented by 1. There are 2 main blocks for the counter-based TDC architecture given in **Figure 2.15**, which are the clock generator and the counter.

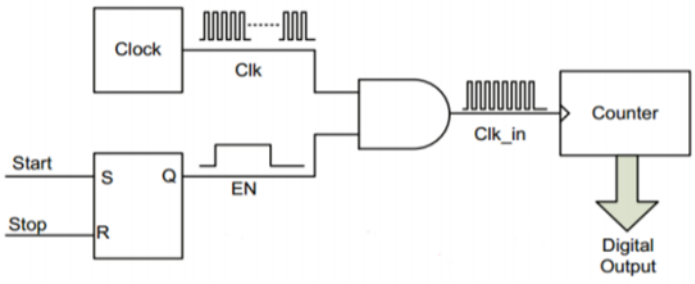

Figure 2.15: Counter-based TDC architecture [68].

Start and Stop signals generate an enable signal via SR latch, and this enable signal is used with an inner clock generator to obtain a counter clock [68]. In this method, the difference between the two input clocks can be represented with the inner clock frequency. For instance, if the frequency generator has a 1 GHz clock, and there is a 2 ns difference between clocks, the counter should give “2” as an output. In terms of resolution, phase error signals will always be the integer multiple of the frequency generator’s period. For high resolutions, the frequency of the clock generator should be increased but the design of faster counters can be challenging. Also, the power

consumption of the clock generator will increase when the output frequency increases. Furthermore, the quality of the generated output highly depends on the phase noise, jitter, and stability of the clock generator [49]. On the other hand, clocks with good spectral purity can be generated via crystal but they increase the cost of the systems as well.

2.2.4.2. Analog-to-digital conversion-based TDC

To avoid the disadvantages of using counters to measure the time difference between clocks, Analog-to-Digital converter-based TDCs can be employed in sub-micron CMOS technologies. These architectures take advantage of the advanced developments in ADC design. Combination of TDCs with SAR, sigma-delta modulation, or pipelined ADC architectures give higher resolutions than the other TDCs even with smaller delay times [69].

ADC-based TDCs work with a principle of multistep conversion. Instead of directly digitizing the phases, the time difference is converted to voltage first, and then the voltage is quantized to digital bits.

ADC-TDC pairs, which are also known as time-to-voltage converter-based TDCs, consists of two main blocks; an ADC and an integrator. In **Figure 2.16**, blocks of the voltage conversion-based TDC are illustrated.

As it was mentioned before, conversion of the time to voltage can be realized with an integrator. Integration of a voltage between specific time instances can be achieved via a capacitor and constant current source pair. Basically, in a time window that is equal to the difference between 2 input clocks, a capacitor is charged with a current source.

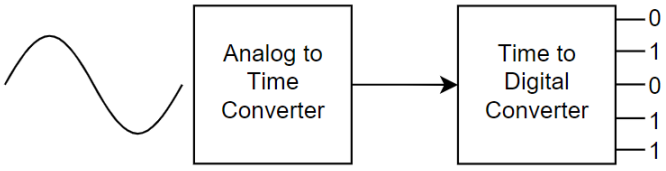

Figure 2.16: Working principle of time-based Analog-to-Digital converter.

After the voltage conversion, the digitization process starts with the ADC. If the working principle in the figure is implemented with Successive-Approximation (SAR) ADCs, resolutions in femtosecond levels can be achieved [69]. The performance of the ADC-based TDCs depends on the type and speed of the ADC and the linearity of the voltage-to-time conversion circuit.

The integrator used in the TDC is generally based on charging capacitors with a current source. These capacitors work in the same manner as charge pumps in analog PLL systems. However, there are also flip-flop-based designs that can be used with extra interpolators [70]. Because of the limited output resistance of the constant current source, linearity degradation may occur during the conversion. Implementing operational amplifier-based integrators was proposed for the solution of the nonlinearity problem [71]. On the other hand, employing op-amps as a voltage-to-time regulator can reduce the digitization speed because of the narrow bandwidth [49]. In **Figure 2.17**, a basic way of voltage-time and time-digital conversion can be seen.

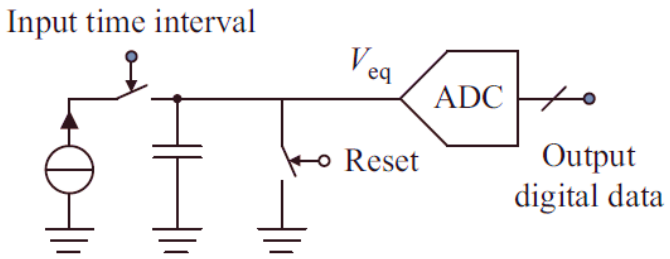

Figure 2.17: ADC based TDC topology [49].

2.2.4.3. Delay-line based TDCs

Instead of counting the phase difference between inputs directly, a delayed version of the reference clocks can be generated to obtain finer resolutions. There are various types of architectures that employ delay lines to obtain propagation.

Flash (Single Delay Line) TDCs

As it was mentioned before, the most significant parameter of the TDC is its resolution. Previous methods can achieve resolutions that are comparable with the incoming clock period. However, the Flash TDC structure employs uniformly distributed delay lines to achieve lower resolutions.

The phase difference between stages can be changed via design architecture and it only depends on the propagation delay between cells [72]. Mainly, 2 types of delay lines are used in TDCs as a known reference: CMOS inverters and CMOS buffers [73]. When an inverter-based line is used, successive delays have opposite signs and overall oscillation goes with a negative-positive coupling [74]. On the other hand, in buffer-based delay lines, the sign of the delay will be always positive or negative. A positive sign means that phase is logic “1” and the negative sign represents a logic “0”. CMOS-based buffers and

inverters are generally limited to a couple of pico-second phase differences between stages. However different topologies such as multi-input and gated delay lines can be used to decrease the delay between stages [75]. The detectable range of the flash TDCs is the multiplication of the number of cells in the delay line and the delay between phases. Flash TDCs have advantages in terms of low latency and simplicity. As it can be seen from **Figure 2.18**, it can be constructed by utilizing two types of elements.

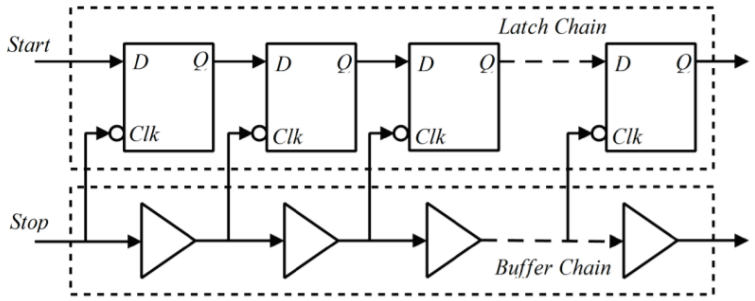

Figure 2.18: Buffer-based Flash TDC [76].

On the other hand, for wider ranges which can be thought of as more bits in the output, the number of the cells in the delay line increases dramatically. Moreover, every single delay between each element should be the same to ensure a linear transfer curve between the phase difference and the error signal. Due to a mismatch between delay-line cells, propagation delay can vary between each element, and it starts to accumulate after each step. At the end of the delay line, accumulation block overflows and the expected output signal cannot be achieved. There are small but significant differences between single delay lines and ring oscillators, and they will be explained in the ring oscillator-based TDCs part.

Vernier Delay Line TDCs

Instead of using a single delay line to obtain an internal reference for measurement between the time difference of the two input signals, the Vernier delay line method utilizes two different delay lines. To achieve finer resolutions, which can be considered as below 10 picoseconds, and to lower the phase noise of the TDC, the difference between propagation delays of two lines is employed. In other words, the Vernier topology was developed to reduce the resolution of the TDC that cannot be decreased via conventional delay line methods in a given technology.

As shown in **Figure 2.19**, two different delay lines, which have a small difference between their propagation delays, should be constructed as an initial step. The common

applications of the TDCs always include two inputs where one of them is coming before the other one. However, Vernier delay lines utilize this phenomenon to calculate the time difference.

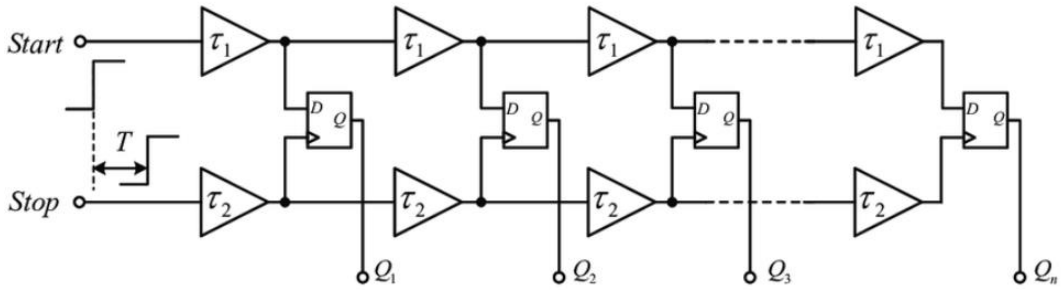

Figure 2.19: Vernier TDC architecture [77].

The first signal is fed to the slower line, which has a bigger propagation delay than the other one, and the second signal is applied to the faster line. After a while registers between delay lines detect the alignment between the delay of the two lines and thermometer-based codes represent the distance between them [78].

Principally, the resolution only depends on the delay difference between the two lines, but the number of stages and mismatch between the propagation delay of each element are also effective on the overall detection resolution.

Furthermore, the main principle of the latency concept behind the single delay line preserves itself for this architecture. Signal still propagates from the first delay element to the last one. The latency is equal to the time that is needed for the alignment of the two signals. Both architectures can utilize buffers and inverters as delay lines, but inside the Vernier topology, two lines should have the same type of delay cells. If not, the probability of mismatch between propagation delays will increase. In contrast to a single delay line topology, due to the finer resolution, vernier delay line architectures achieve the detection of the same time interval with more delay elements [49]. In other words, for wider capturing ranges, the area of the vernier delay lines is significantly larger than single lines. Moreover, since they use more cells, the power consumption of the vernier TDCs is larger than the single delay lines. In conclusion, there is a trade-off between area and resolution in Vernier topology.

2.2.4.4. Ring Oscillator based TDCs

Ring Oscillators can be directly implemented into any kind of TDC architecture as an internal reference clock generator. Fundamentally, ring oscillators utilize CMOS

inverters or buffers as a delay element and the last one feeds the input of the first cell. This configuration can be analyzed further in **Figure 2.20**.

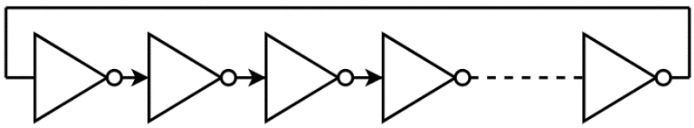

Figure 2.20: Common Ring Oscillator topology.

Basic Ring Oscillator based TDCs

Instead of using the propagation of the signal in one direction, which is from the first element to the last one, ring oscillators can be utilized to achieve multi-propagate signals. In this configuration, propagation of the signal continues until the measurement is completed. In other words, without using an excessive amount of the delay cells, conversion can be completed with a smaller number of cells. There are different parameters for ring oscillators that affect the quality of the module. These types of TDCs are the same as the single delay line architecture with small differences. The resolution of the conversion is directly related to the propagation delay of each cell. However, ring oscillators should use an "odd number" of inverters to keep oscillation going. On the other hand, this requirement is not valid for buffer-based ring oscillators. Also, the frequency of the basic ring oscillators can be calculated with delay and the number of stages via equation **2.2** [79], [80].

$$f_{osc} = \frac{1}{2N \, x \, t_d} \quad \textbf{(2.2)}$$

N is the number of stages of the ring oscillator and t_d is the propagation delay between each cell. However, voltage swing, current consumption, and temperature directly affect the frequency of oscillation [80].

High frequencies and low propagation delays can be achieved with basic RO configuration. On the other hand, single input, single output delay cells have limited minimum delays even in smaller CMOS technologies. However, for applications that require finer delay values, there are more advanced solutions. Employing one of these solutions may be needed for these applications because the delay between elements directly determines the resolution of TDC.

After building the ring oscillator, a reference phase should be chosen for counting operation in the basic RO structure. The counter increases its output by 1 for each full

cycle of this reference phase. In other words, the counter starts to evaluate the time difference between the two inputs, by counting the reference cycles [81]. However, the reference signal acts as an enable and the feedback signal acts as a disable through the process.

The measured time difference for the circuit in **Figure 2.21** can be calculated as shown in equation **2.3**;

$$T_{Measured} = \left(TA_{Feedback} - TA_{Reference}\right) \times PD + (OUT \times T_{RO}) \qquad \textbf{(2.3)}$$

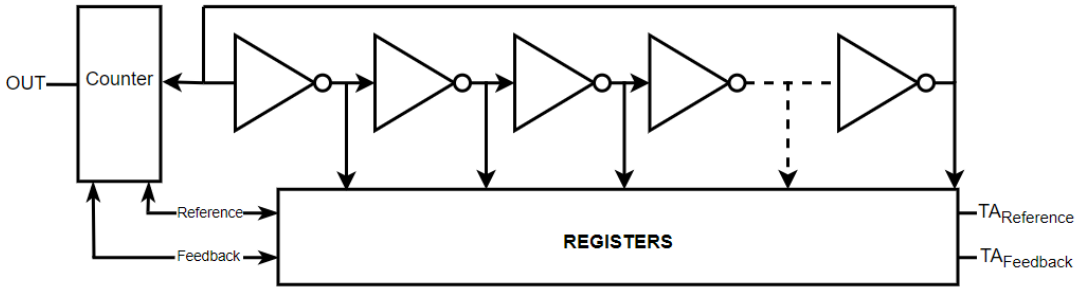

Figure 2.21: Ring Oscillator based TDC.

The principle behind the operation is representing the time difference by delay and the output of the counter. So, TA is the arrival time of the signals, PD is the propagation delay of each delay cell and OUT is the output of the counter. Furthermore, TRO is the period of the reference phase. The first term of the summation gives the fine result and the second one shows the coarse difference between signals. In other words, the term on the right-hand side can be considered as the number of full cycles in the RO and the left part is the representation of the difference in a single cycle.

Employing the same delay cells in each cycle makes the dynamic range of the ring oscillator theoretically limitless. However, because of the output range and the working frequency of the counter, there should be some upper limit for the detectable range. One of the most unfortunate disadvantages of ring oscillators is power consumption. Since there is a continuous and stable oscillation, the power dissipation of the system is much more than the single-delay line architecture.

Vernier Ring Oscillator based TDCs

Instead of using delay-line topology, the Vernier ring TDC architecture utilizes two ring oscillators to generate fine delays between each oscillator, and for larger time differences, the same delay cells can be re-employed. The working principle of the ring oscillator-

based vernier TDCs is the same as conventional Vernier ones. When the first signal, which is also known as reference or lead signal, comes, the delay line starts to oscillate through the slow delay ring. After the second signal is applied, it is automatically directed to a fast oscillator, and the system starts to wait for detection of the alignment. When alignment occurs, a comparison of the phases of the signals is done and the difference is represented with a thermometer code. RO-based Vernier TDCs provide wider detectable ranges without using an excess amount of delay cells [82] and the block diagram for this topology is presented in **Figure 2.22**. Also, the resolution still depends only on the propagation delay difference between slow and fast delay-rings. In other words, the same resolution and wider capture range can be achieved in a smaller area. Furthermore, the propagation delays of the two ring oscillators should be close to increase the resolution.
The dynamic or capture range of the Vernier RO-based TDCs depends on the number of delay cells in the RO. But the most significant parameter that can augment the range is increasing the number of bits of the loop counter.

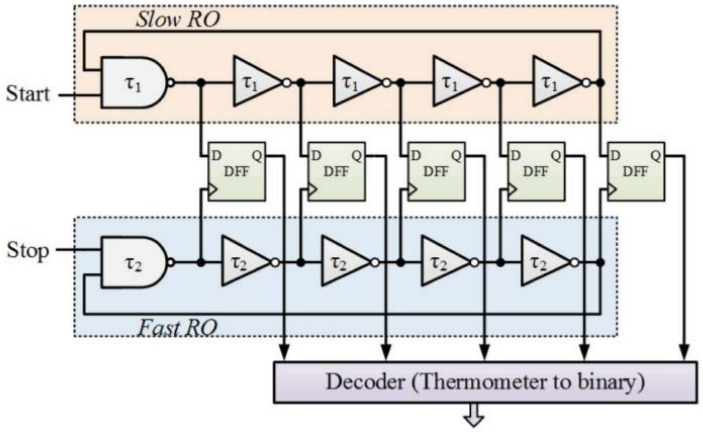

Figure 2.22: Vernier Ring Oscillator based TDC Topology [82].

Multipath Ring Oscillator based TDCs

One of the most known drawbacks of the basic RO structure is limited resolution. As it was mentioned before, single-input-single-output (SISO) delay elements have a lower limit for the propagation delay, which is independent of technology [83]. There are various ways to solve this issue, and one of them is employing a multipath ring oscillator structure. Utilizing this method improves the resolution of TDC several times without changing the power consumption. To apply these kinds of structures, the gates of the PMOS and the NMOS of the inverter are controlled by different inputs, and the configuration is illustrated in **Figure 2.23**.

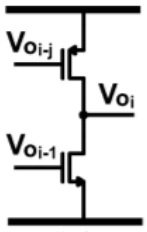

Figure 2.23: 2 Input inverter configuration [75].

For instance, as it can be seen from **Figure 2.24** that the output of the 2nd delay cell feeds the NMOS input of the 3rd cell, as well as the PMOS input of the 5th cell.

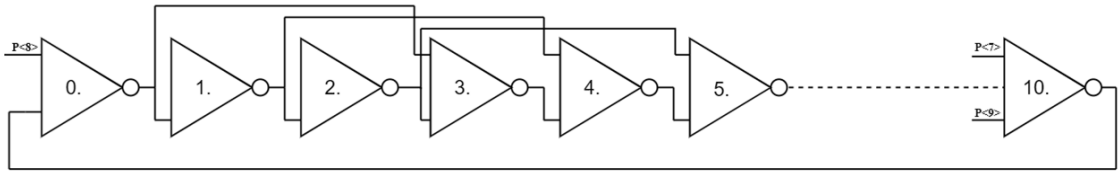

Figure 2.24: 11 Phases multipath Ring Oscillator.

This configuration allows the early evaluation of the PMOS input, which has slower carrier mobility than NMOS transistors. However, applying the previous inputs to the PMOS ensures the balancing between the speed of transistors. Moreover, two NMOS and one PMOS transistor can be utilized as given in **Figure 2.25** to speed up the overall transition time and this increases the resolution of the TDC even further [84].

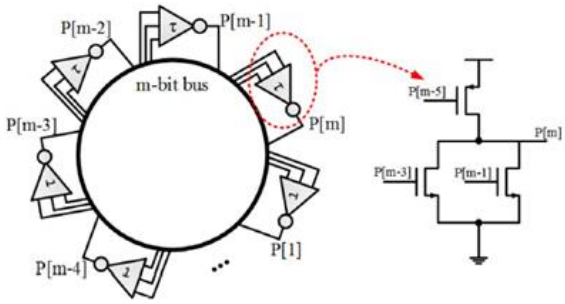

Figure 2.25: Alternative topology for Multi-Input Inverter [45].

In this approach, the designer needs to be careful to apply the correct phase to the correct transistor in order not to break the oscillation. As the resolution of the ring oscillator increases, the resolution of the time-to-digital converter also increases. On the other hand, as with the previous topologies, the dynamic range of the measurement is limited by the output of the counter. Employing multipath ring oscillators can improve the resolution up to a couple of picoseconds [85].

Gated Ring Oscillator based TDCs

The low-resolution problem of the basic ring oscillator can be solved via multipath ring oscillator topology, but the power consumption problem still continues. To solve this issue, the most famous method is gating the delay cells.

There are various ways to implement gating of the cells and they have advantages and disadvantages among each other. The first one is employing MOS switches in line with the VDD and VSS lines [86]. This basic trick prevents the flow of an excessive amount of current in the ring oscillator. When switches are closed, delay cells start to work and oscillation propagates between cells. However, if the switch is open, there will be no current from VDD to delay cells and the overall ring oscillator will be off-state. In fact, in order to guarantee the start of oscillation, applying an initial condition to any of the phases in the ring oscillator is necessary. Without the forced initial phase, which can be "0" or "1", the ring oscillator may not start to oscillate by itself.

There are other gating options without using external transistors. The first delay cell can be replaced with multi-input gates such as Nand or And gates [87]. Nand gate provides an additional condition to start oscillation which can be a start signal or enable as given in **Figure 2.26**.

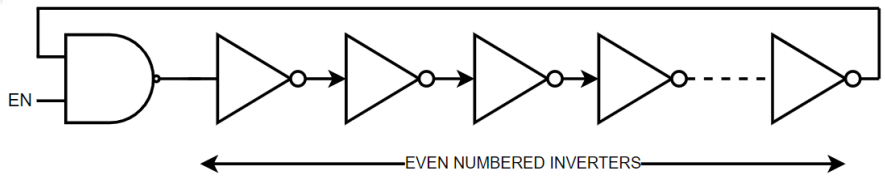

Figure 2.26: Gated Ring Oscillator with Nand gate.

Once the start oscillation starts, the Nand gate acts as an inverter in the oscillator. On the other hand, the propagation delay of the Nand gate should be adjusted precisely to match the delay of the inverters in order to maintain the linearity of the system. In another aspect, the design of the Nand gate is also important for the resolution of the system.

Another conventional method for gating is to employ multiplexers before the input of the delay elements. As it is shown in **Figure 2.27**, this architecture uses an enable signal as the selection bit of the multiplexer. The selection bits of all MUXs are connected to the power line, but the first multiplexer selects its input according to the enable signal. When enable signal is "1", the system starts to oscillate like all the other ring oscillators. However, when enable becomes "1", the system resets itself and becomes gated off.

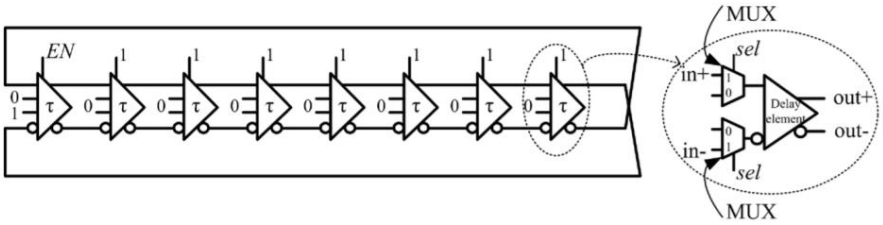

Figure 2.27: Gating Ring Oscillator with Multiplexer [88].

The advantages of the gated ring oscillator topology are not restricted to low power consumption. The first-order difference operation during the measurement of the time difference provides a first-order noise shaping in frequency. Also, the negative effects of cell mismatches can be reduced via this operation as well [75]. In other words, the flat distribution of the noise is transformed to the first-order shaped noise floor, and the results of this phenomenon can be examined in **Figure 2.28**.

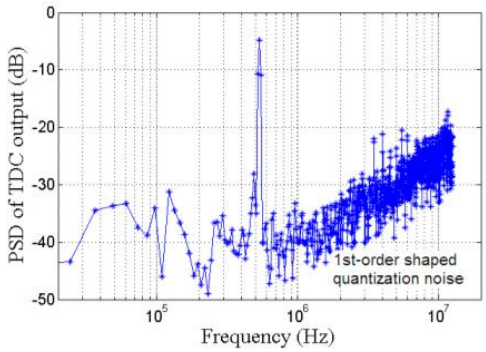

Figure 2.28: First order noise shaping effect of Ring Oscillator [86].

2.2.4.5. 2-D Vernier based TDCs

Like all the previous ring oscillator-based TDCs, also 2D vernier topology employs delay lines or ring oscillators in order to achieve higher resolutions in a small area. However, its novelty is originated from its working principle and wider detectable range [89]. Also, the required time for the calculation, which is also known as latency, of the phase difference is significantly reduced via improved 2D-Vernier topologies [90].

To create the fine difference between upcoming signals, delay lines or ring oscillators should be placed perpendicularly to compare every single phase with others. To ensure equivalent delay between each comparator, generally, capacitor banks between delay elements or dummy cells are employed at the corner of the Vernier plane as in **Figure 2.29** [91].

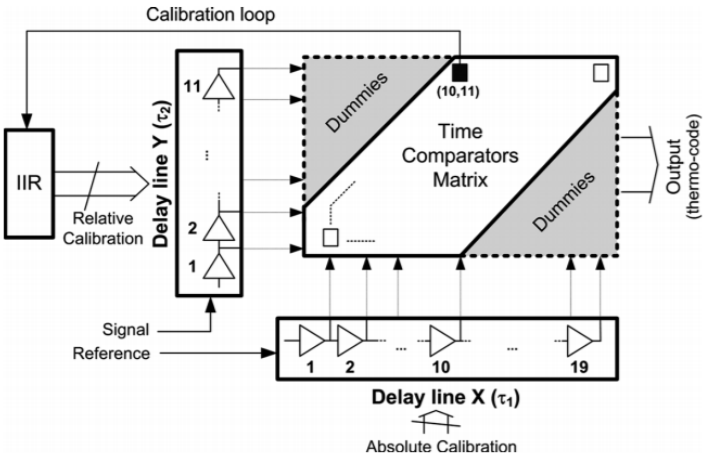

Figure 2.29: 2D Vernier TDC topology [91].

Because of the two-dimensional comparison between each delay, many results are obtained, and they should be mapped to correct addresses. In other words, when the alignment occurs, the corresponding vector should be determined. To provide this logic, column selectors can be utilized [90]. Besides all its advantages, some studies [92] proved that 2D-Vernier architecture also provides second-order quantization noise shaping as well.

In state-of-the-art technologies, 2D-vernier architecture can achieve a couple of picosecond resolutions in a wide dynamic range [93]. Nevertheless, to ensure low power consumption and high linearity, 2D-Vernier architecture can be utilized with gated ring oscillators and multiphase counters [92].

2.2.4.6. Time amplifier based TDCs

Instead of utilizing simple buffer & inverter-based delay lines for the referencing, amplifier type cells can be employed for quantization of the time difference [94]. This method basically takes the time between 2 phases and amplifies it to ease the detection. The amount of the amplification should be the same between each element to prevent any nonlinearity at the transfer curve. The principle behind the time amplification is the same as the voltage amplification in the pipelined ADCs [95]. To decrease the tension on the next comparator and to facilitate the quantization process, the analog voltage of the previous stage is amplified before any progression. However, there are still some application-based differences between voltage amplification and time amplification. There are many methods for increasing the time difference between two distinct events. Latch-based designs [96] as given in **Figure 2.30**, or integration-based time stretchers that utilize pulse trains [97] can be valid examples that have good resolution. On the other

hand, because of the narrow dynamic range of the time amplification-based TDCs, the measurable time difference is much lower than the conventional methods [49].

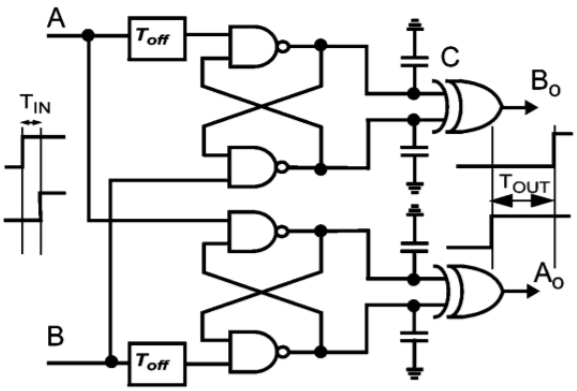

Figure 2.30: SR Latch-based Time Amplificator circuit [98].

2.2.4.7. Two-step TDC circuit

In order to increase the resolution of the TDC, utilizing two steps can be a useful method to resolve the time difference. To achieve higher resolutions in this topology, the number of bits for each stage should be determined first [97]. Also, there should be different ring oscillators or delay lines to obtain coarse and fine resolution values. Mainly, the first part of the TDC measures the coarse distance and the second part calculates the remaining fine distance between input signals [99]. Generally, the delay of the steps is adjusted to be integer multiples of each other. For instance, the propagation delay of the course stage can be 4 times larger than the steps of the fine stage [100].

The resolution of the system directly depends on the delay between each element. However, conversion speed can be low due to the usage of selectors and buffer delays between the TDC steps.

2.2.4.8. Multi-step TDC circuit

The working principle behind the two-step TDC architecture can be employed to form a multi-step TDC as well. The total number of bits in TDC is divided by the number of stages and a selection circuit is employed between each stage. The last step of the architecture consists of TDC and all previous outputs were concatenated to form the final result. The analogy behind the multistep circuit can be investigated further in **Figure 2.31**.

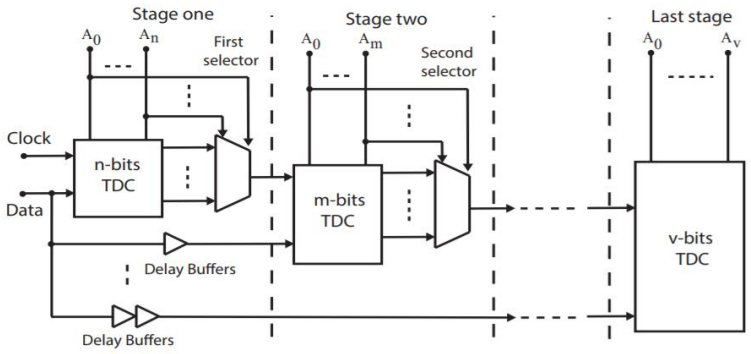

Figure 2.31: Circuit Diagram of Multi-Step TDC [100].

There are non-negligible characteristics that need to be considered before designing a multistep TDC. To meet specific requirements such as the different resolutions between stages, the number of delay cells should be multiple of each other between steps. Moreover, for each step, there will be different registers to record the phase of the oscillators and the total number of them can be 2^N-1 [100]. As it is seen, if the dynamic range of the system is high, the number of the required number of registers grows exponentially. However, some solutions employ latches instead of flip-flops, which decreases the power consumption and area [101].

2.2.4.9. FPGA based TDCs

Instead of developing a new TDC in an integrated circuit, field-programmable gate arrays (FPGA) can be utilized for digitization of time. In other words, FPGAs can be preferred instead of ASICs. There are many advantages of FPGA-based TDCs in terms of cost and effort [102]. Because of the short development time, using FPGA is a cheaper and faster solution for many applications, especially for digital ones. Moreover, all FPGAs include inverters and buffer lines, which can be used for fine interpolation of time differences [103].

Furthermore, FPGAs provide programmability to TDCs, which can facilitate the development and error correction process. Also, structures of the FPGAs allow utilization of TDCs for multichannel purposes. On the other hand, there are some disadvantages of FPGA-based TDCs compared to ASIC-TDCs in terms of linearity. Because of the inner structure and design methodologies of FPGAs, there can be some clock skewing and carry chain nonuniformity problems [104]. These problems eventually lead to some Phase noise and nonlinearity issues that can distort the performance of the TDC. However, some of the architectures like dual-phase [105] and tuned-TDL [106] were proposed to solve the nonlinearity of the FPGA-based TDCs. **Figure 2.32** illustrates a valid example for tuned

TDL topology in FPGA. However, each sub-TDL is averaged to form the final output and decrease the nonlinearity.

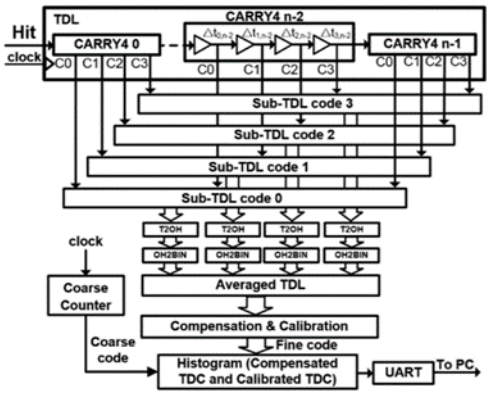

Figure 2.32: Tuned-TDL structure in FPGA-based TDC [104].

Like all the other TDC topologies, the resolution of the FPGA-based ones is critical and directly related to the propagation delay between each cell in the delay line. However, almost all FPGA-based TDCs employ tapped delay lines to get successive propagation of an incoming phase with a specific delay. The finest resolution of the TDC can be increased via employing two different delay lines or ring oscillators in Vernier topology. There is no significant difference between ASIC and FPGA-based vernier topologies in terms of function and circuitry.

In addition to nonlinearity problems, FPGA-based TDCs suffer from the area and supply problems. Principally, the propagation delay should not vary when the supply voltage or current changes [107]. Hence, maintaining the same value and performance is a significant problem for FPGA-based designs. Also, the applicability of the TDCs to higher frequencies is hard with FPGAs because of their relatively low working frequencies compared to the ASIC-based ones. Moreover, FPGA-based designs are not optimized for the small area since a large overhead of gates exists in them. Lastly, temperature dependency of the resolution and stability is another common problem that can be encountered in FPGA-based TDCs [108].

2.2.4.10. Algorithmic TDCs

Principally, algorithmic TDCs work in a similar manner as the time to amplitude converters except for how it performs the amplification of the phase between the two clocks. In algorithmic TDCs, amplification of the phase error was realized by changing the frequency of the ring oscillators. Instead of decreasing the difference between phases step by step, the residue is amplified and digitized with the same delay for each iteration.

One of the most famous studies that use algorithmic TDCs is able to achieve a couple of picosecond level resolutions [109] by employing a multipath ring oscillator. The oscillation frequency of the ring oscillator is controlled by current limiting switches used in the oscillator to change the delays of the cells [110]. **Figure 2.33** shows an algorithmic TDC architecture that employs 2 different counters, which count the full cycle of the ring oscillator and the reference clock separately.

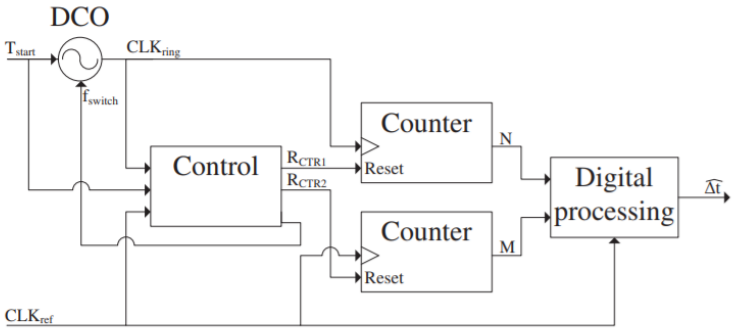

Figure 2.33: Algorithmic TDC architecture [109].

When the start signal comes, the ring oscillator starts to work with fast frequency until the reference clock comes to initiate the tuning process. Consequently, the controller makes the oscillation slower to ensure the alignment between the two signals. The final resolution of the overall TDC is determined by the ratio of the ring oscillator's operating frequencies. The key tradeoff in this architecture is deciding between the speed of measurement and the resolution. Moreover, increasing the ratio between fast and slow frequencies will increase the contribution of the ring oscillator's phase noise to the overall noise of the system [109].

CHAPTER 3

3. EXPERIMENTAL PART

3.1. The proposed TDC architecture

In this thesis, a Time to Digital Converter was designed for an All-Digital phase-locked loop (ADPLL) with 180nm CMOS XFAB technology. As with all the other topologies, the fundamental purpose of this TDC is also to measure the time difference between phases of two clocks which are Reference and Feedback (Divider) clocks. On the other hand, instead of obtaining the overall difference in a single step, the evaluation process is separated as coarse and fine measurements in order to increase the resolution of the system and to decrease the area of design. In other words, to balance the area and the resolution of the architecture, a hybrid topology is utilized. To build the top-level schematic, previously prepared standard cells were employed.

To create a “known” time interval, a multipath gated ring oscillator was constructed first, and phases are utilized to calculate the fine difference between the two inputs using Hamming distance modules. The reference phase, which is the zeroth (0.) phase of the ring oscillator is also counted for each input to obtain a coarse value. Eventually, fine and coarse differences are summed up to get TDC phase error between clocks. Details of the modules are presented in the next sections. The overall architecture of the proposed TDC is shown in **Figure 3.1**.

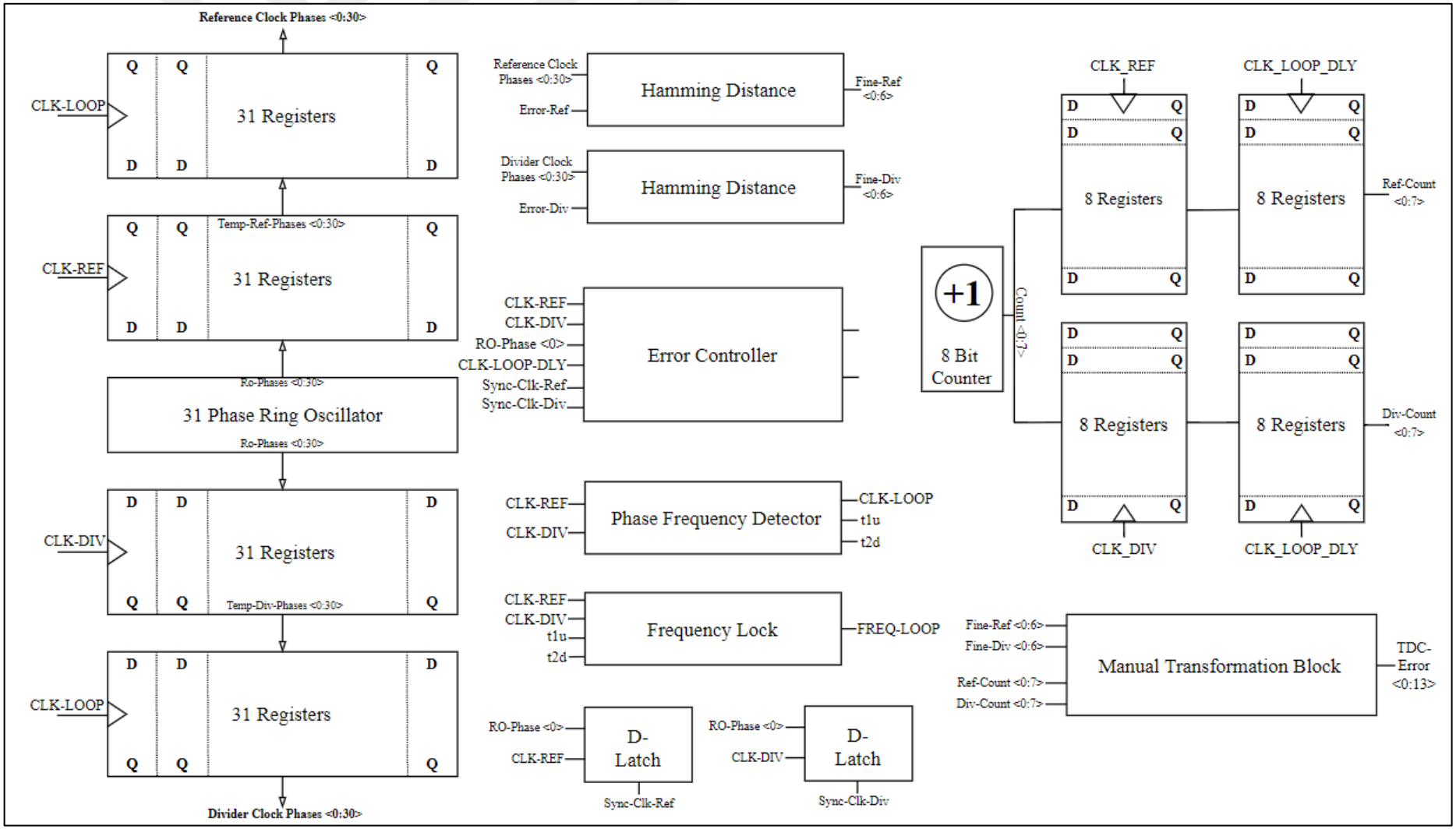

Figure 3.1: Overall architecture of the proposed TDC

3.2. Ring Oscillator

The first step of the design process is building a reference oscillator that creates a "known" phase difference. As it was mentioned before, single-input single-output inverters were tried first but unfortunately, a 40 ps delay was achieved at best, which is not adequate for this project. To decrease the delay down to 20-25 ps band, a multipath ring oscillator topology was implemented with 31 inverters. Achieving low delay between phases is very important since this eventually determines the resolution of the TDC. The frequency and number of delay elements in the ring oscillator are inversely proportional to each other. In other words, to decrease the frequency, the number of stages should be increased in the same propagation delay. The relationship between delay elements and frequency is demonstrated in equation **3.1**.

$$PD = \frac{1}{2N \; x \; f_{RingOscillator}} \tag{3.1}$$

PD is the propagation delay between the inverters, and it can only be adjusted with the transistor sizes. N is the number of inverters that are employed to build a ring oscillator and it is the only way to decrease or increase the frequency of oscillation.

$$f_{RingOscillator} = \frac{1}{62 \; x \; 22.18 \; x \; 10^{-12}} \tag{3.2}$$

When 22.18 ps is chosen as the propagation delay and the number of stages is set to 31, 727.2 MHz frequency was obtained for oscillation as is shown in equation **3.2**. This delay number was chosen as a reasonable value for the process since designing higher-speed counters is not easy to realize in 180 nm technology. Moreover, to obtain a 22.18 ps propagation delay between each stage output, a multiphase ring oscillator topology was constructed. In **Figure 3.2**, the device size of the inverters used in the ring oscillator is shown.

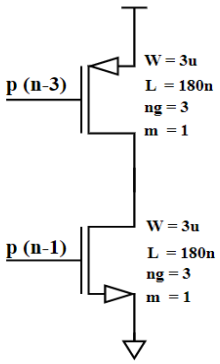

Figure 3.2: Transistor sizes of Ring Oscillator's inverters.

The overall configuration of the ring oscillator is given in **Figure 3.3**. To show the multipath connections, blue and red lines were used.

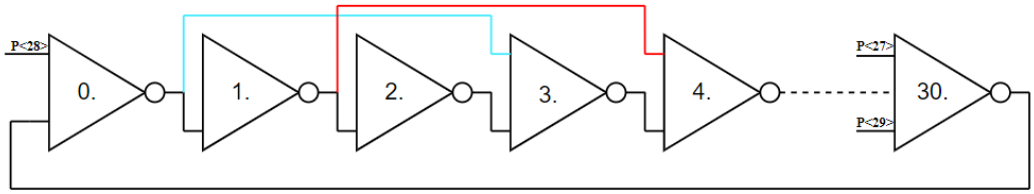

Figure 3.3: Multipath Ring Oscillator architecture.

When the blue path is tracked, it can be seen that the output of the 0th inverter is applied to the gate of the NMOS transistor of the first inverter. Besides, it also drives the PMOS input of the 3rd inverter. Similarly, the same methodology is used for every single inverter and another connection is shown in the red line. For generalization of the wiring process, it can be said that the gate of the NMOS should see the output of the previous stage which is equal to P <n-1> where n is the current stage. On the other hand, P<n-3> should be connected to PMOS, to balance the speeds of transistors and eventually decrease the propagation delay. However, to initiate the oscillation, and reduce the power consumption of the ring oscillator, a big PMOS switch was employed in series with the supply. As a result of using this power gating switch, the ring oscillator does not consume any power when it is disabled.

Furthermore, to determine the bandwidth of the digital low pass filter, the quantization noise of the TDC should be calculated. Equation **3.3** [111] is valid for ring oscillator-based TDCs and it is employed to calculate quantization noise for different PLL outputs and reference frequencies and, results were presented in the "Results and Discussion" section.

$$S_{\phi_{out}}(f)_{TDC} = \frac{1}{T} \times |2\pi NG(f)|^2 \times \frac{\Delta^2{}_{RO\_delay}}{12} \quad \textbf{(3.3)}$$

Quantization noise is directly related to the "N", which is the ratio between PLL output frequency and the reference input frequency. 1/ T is the frequency of the reference signal which is one of the inputs of the TDC. Furthermore, the propagation delay of the Ring Oscillator which is Δ_{RO_delay}, also another significant parameter that affects the noise of the system. As is expected, if the resolution of the TDC increases, the noise of the digitization process decreases. Moreover, 2πN is the DC gain of the proposed TDC and in low frequencies, G(f) is equal to "1".

3.3. D-Flipflop array for fine difference

To obtain continuity in the fine measurement of the TDC phase error, phases of the ring oscillator should be registered for each cycle. In order to meet this requirement, 31 different D-Flipflops were utilized in a parallel fashion. Besides, another D-Flipflop array had to be used to adjust the release time of phases. In other words, phases will be caught and released with different and predetermined clocks.

As can be examined from **Figure 3.4**, each element in the D-Flipflop array has a common clock, but each sub-unit has different D and Q ports. Moreover, each register is triggered at the rising edge of the input clock and reset at the falling edge of the reset bit. Register arrays utilize Reference and Divider Clocks to catch phases and they release them with Loop Clock which is the output of the Phase-Frequency Detector module. In **Figure 3.4**, the working principle of the catching and releasing mechanism of phases can be seen.

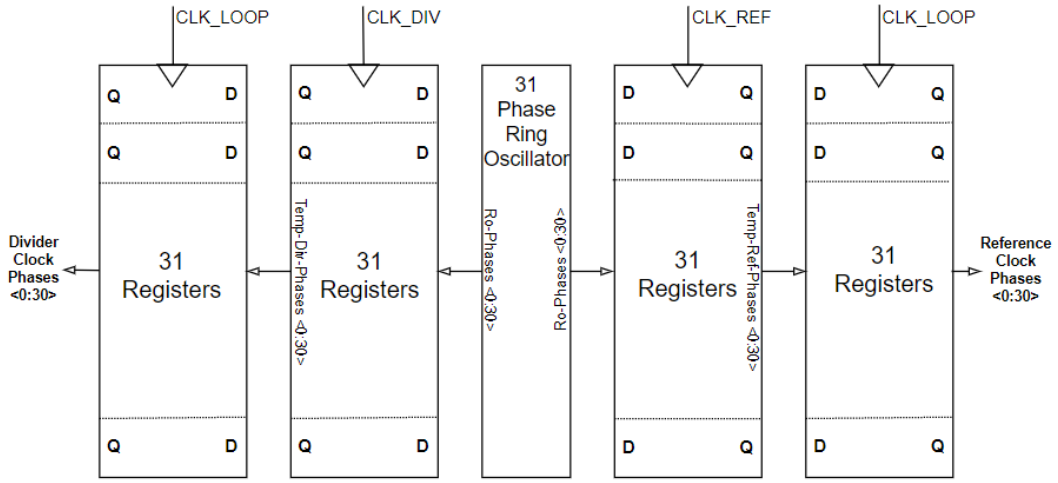

Figure 3.4: Block diagram of the D-Flipflop array of ring oscillator phases.

To build up this architecture for 2 different clocks and, 4 different register arrays were implemented, which means, 124 D-Flipflops were employed in total.

3.4. Hamming Distance

Hamming Distance module basically takes 31 phases from ring oscillator and it compares with a predefined reference phase. The output of this module is used for a calculation of fine distance and it is represented with 7 Bits. TDC in this work uses the 0^{th} Phase of the ring oscillator, which is equal to

(P<30>MSB) 010_1010_1010_1010_1010_1010_1010_1011(P<0> LSB), as a reference to calculate the difference. The main function that calculates the final output is basic XOR operation and summation. The incoming phase is XORed bit by bit with the reference first, then these 31 different XOR outputs summed to get the primary distance. Furthermore, a basic logic was also constructed to differentiate LSB=0 or LSB=1 issue and external error input. LSB problem can be explained as obtaining the same distance result for both LSB=1 and LSB=0 conditions. To prevent this phenomenon, if the incoming phase starts with "0" then the primary result will be subtracted from 62. Here system uses 62 because even though we have 31 inverters and 31 phases; 1 full cycle of oscillation includes only half of the phases. In other words, 1 period (from 0 to 0, or 1 to 1) can be represented with 62 phases. For instance, if the second phase of the ring oscillator is "0" initially, when a single full cycle is completed in the ring oscillator, it will be "1" and after the second deviation is completed it will be "0" again. Moreover, if the system has an error, the primary result will be extracted as a negative number to prevent sudden jumps at the output of the TDC. **Table 3.1** is the easiest way to demonstrate the function and conditions of the hamming distance block.

Table 3.1: An example for calculations in the Hamming Distance Block.

Conditions	Reference Phase	Incoming Phase	Final Distance
LSB=1	01010101010101010101010101011	01010101010101010101010110101	4
LSB=0	01010101010101010101010101011	10110101010101010101010101010	58
Error=1	01010101010101010101010101011	10110101010101010101010101010	-4

Normally, the first and second incoming phases should give the same results at the output because summation results are the same. However, in terms of distance, they should not be equal. As it can be seen from the table above, the second condition has "0" in LSB and the final result is subtracted from 62. Error condition depends on error input and the 28th phase of the ring oscillator. This phase is important because it indicates the order of toggling. **Figure 3.5** demonstrates the working principle of the Hamming Distance module.

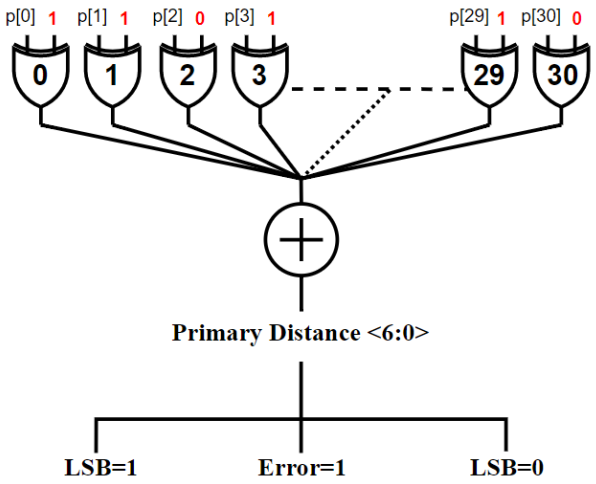

Figure 3.5: Working principle of the Hamming Distance block.

After modifications, and conditioning the system with LSB and Error, the output was designed as 7-Bit, and MSB shows the sign of the final distance. Hamming Distance Block was utilized for both Reference Clock and Feedback Clock to understand their fine differences with respect to the common phase.

3.5. D-Flipflop array for coarse difference

Counter results also need to be registered and held until the counting process of the number of full cycles in the ring oscillator is finalized. Both Reference and Divider Clocks have their own counter values and these numbers are registered at the rising edges of these clocks. Moreover, D-Flipflop arrays drive other register arrays which will be triggered with the delayed version of the Loop Clock. In other words, temporary counter results for each clock will be released simultaneously when the delayed Loop Clock comes.

Counter in this project has an 8-bit output and to catch these bits, 8 different D-Flipflops were utilized in a parallel fashion. Subsequently, another D-Flipflop array consists of 8 registers that are used for releasing mechanism. When this configuration is used for two input clocks, the system employs 32 D-Flipflops in total. Additionally, each register in an array has the same clock and different D & Q ports as well.

In **Figure 3.6**, the working principle of the counter logic was demonstrated.

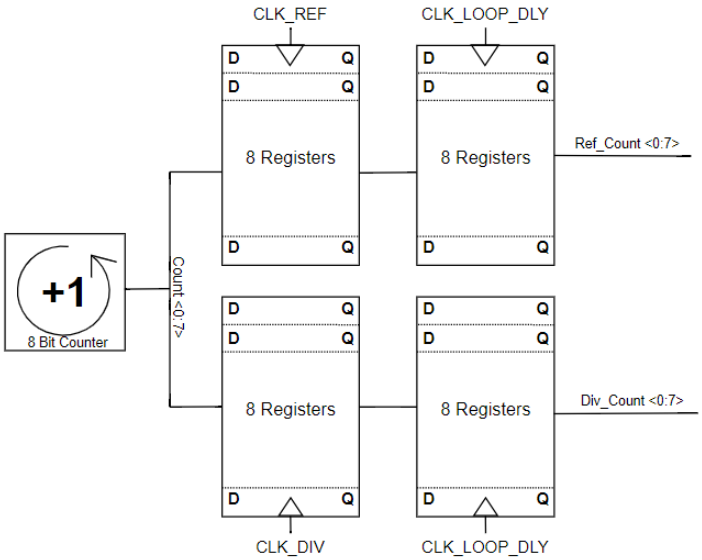

Figure 3.6: Block diagram of the D-Flipflop array of counter outputs.

A digitally synthesized 8 Bit counter was employed to count the initial (0^{th}) phase of the ring oscillator. The most important parameter for the counter is handling the speed because it works in 700-1000 MHz interval. To ensure this requirement, the counter was synthesized with Cadence using previously prepared Standard Cells. Maximum and Minimum Delays were checked from slack time reports and no negative delay was obtained. In other words, slack time violations were prevented via decreasing the frequency of the operation and strong buffer trees. The resultant bits of the counter were used as a coarse distance for specific clocks.

3.6. Manual Transformation block

The main block for this project is the Manual Transformation Block, which calculates and constructs the final result of the top module. Inputs of this block are the outputs of the D-Flipflop arrays for counter and hamming distance blocks. As an initial step, the difference between fine distances of Reference and Divider clocks was calculated. After that, to balance bit numbers, the results of subtraction were elongated to 14 bits and saved for other steps. Secondly, the difference between two counter results subtracted to achieve a coarse difference between input clocks and then elongated to 14 bits. As it was mentioned before, 1 period of the ring oscillator is equal to a 62 phases difference. In other words, 1 coarse distance is equal to 62 fine distances, and to convert the coarse

distance to a fine one, the elongated difference was multiplied by 62.

As a final step, previously processed fine and coarse distances were summed up to obtain the final 14-Bit TDC phase error. The Reference Clock can be 20 MHz or 10 MHz in the proposed PLL, and the dynamic range of the TDC should be determined according to these values. The reason behind the selection of 14 Bits as output is to provide sufficient range for the measurement process even for the 10MHz reference. 14 Bits are able to represent a phase difference between -180 ns and 180 ns, which gives a phase error between -8192 and 8192.

In **Table 3.2**, examples that will facilitate the understanding of the working principle of the block are presented.

Table 3.2: Example for the Manual Transformation operation.

	Reference Clock	**Divider Clock**
Fine Distances	0001011 (11)	0101001 (41)
Elongated Fine Difference	00000000011110 (30)	
Coarse Distances	0010001 (17)	0111000 (56)
Coarse Difference	00000000100111 (39)	
Transformation of Coarse to Fine	00100101110010 (2418)	
Sum	00100110010000 (2448)	

The fine difference between reference and divider clocks is equal to 30, and the difference between coarse distances is equal to 39. When the coarse difference is transformed into a fine difference by multiplying it 62, 2418 was obtained. If we sum coarse and fine differences, the overall result needs to be equal to 244. This overall phase locking process should be maintained in PLL until reaching "0" phase error between input clocks.

Figure 3.7 shows the block diagram for the working principle of the Manual Transformation Block.

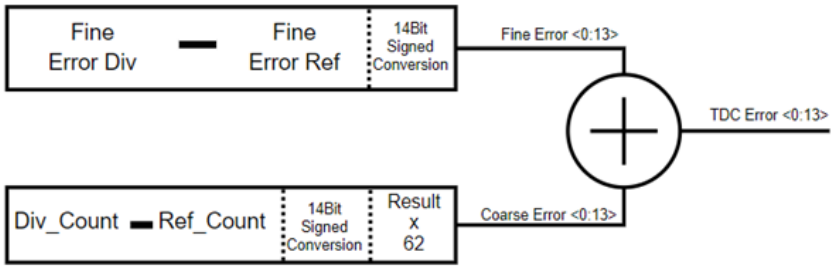

Figure 3.7: Working principle of Manual Transformation Block.

3.7. Phase-Frequency Detector

Phase Frequency Detector utilizes 2 inputs to generate a pulse to control the initiation of the final error calculation. When the reference clock comes, the “t1u” signal becomes “1” inside of the PFD. Also, when the Divider clock comes, the “t2d” signal becomes “1” and these signals are combined to get a pulse which is labeled as Loop Clock. The main purpose of this signal is to regulate and maintain the continuity of the measurement of the phase error. Moreover, intermediate signals, “t1u” and “t2d” are used in the Frequency Lock module. **Figure 3.8** demonstrates the block diagram schematic of the phase-frequency detector.

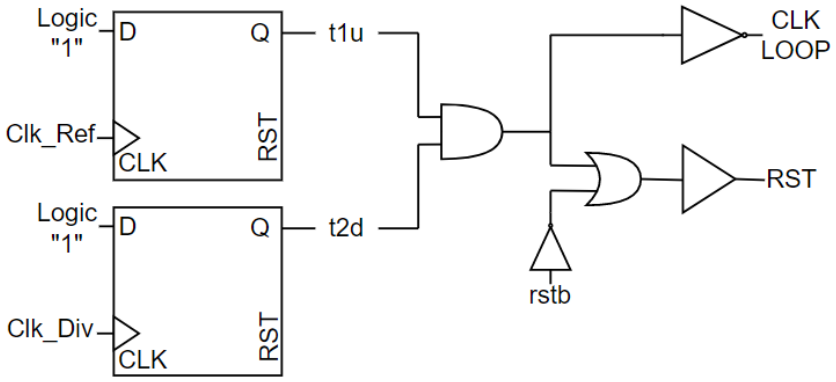

Figure 3.8: Block Diagram of the Phase Frequency Detector.

The t1u signal is triggered to become “1” at the rising edge of the reference clock. Also in the same manner, at the rising edge of the Divider Clock, the t2d signal becomes “1”. Furthermore, the creation of an internal reset inside the PFD block is one of the most significant milestones for this module. Its normal state is logic “0” but when both clocks come, it becomes 1 and resets the system to get Loop Clock pulse. After a “1” ns delay, it turns back to “0” and waits for another input clock. In other words, PFD is nothing but a pulse generator that works with incoming clock signals. **Figure 3.9** presents simulation results for the signals and logic levels inside the phase-frequency detector.

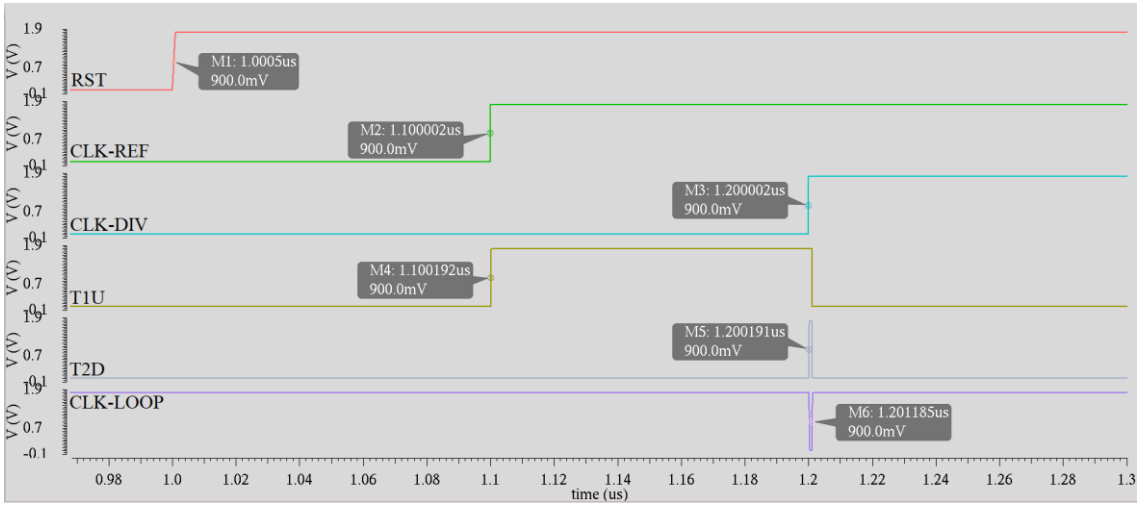

Figure 3.9: Example output for the PFD module.

First of all, after the RST bit initiates the system, PFD waits for the first clock input. Then, Reference Clock comes at 1.1µs and triggers the T1U signal to "1" after a 190 ps delay. When Feedback Clock comes, the T2D signal becomes "1" at 1.2 n and the internal reset bit refreshes inner blocks. At the same time, Loop Clock becomes "0" and waits for 1 ns to be "1" again. Finally, all signals return to their initial conditions after the generation of the loop clock successfully.

3.8. Frequency Detector

Frequency Lock output is not significant for TDC itself but, it is very important for the DCO in an All-Digital PLL. It controls the transition between the coarse and fine-tuning of the DCO. Mainly, this module consists of two registers and one "NOR" gate to obtain Frequency Lock output. Previously created "t1u" and "t2d" signals in PFD were utilized with incoming reference and divider clocks. The schematic of the module is presented in **Figure 3.10**.

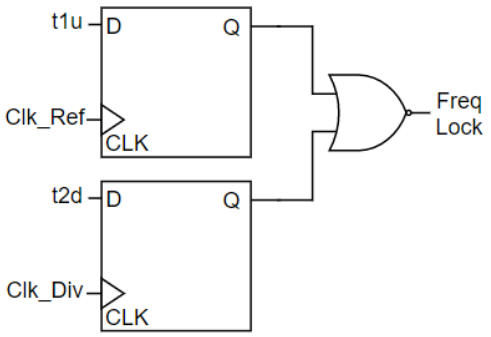

Figure 3.10: Block diagram of the Frequency Lock module.

Simulation results of the main signals and logic levels can also be seen in **Figure 3.11**.

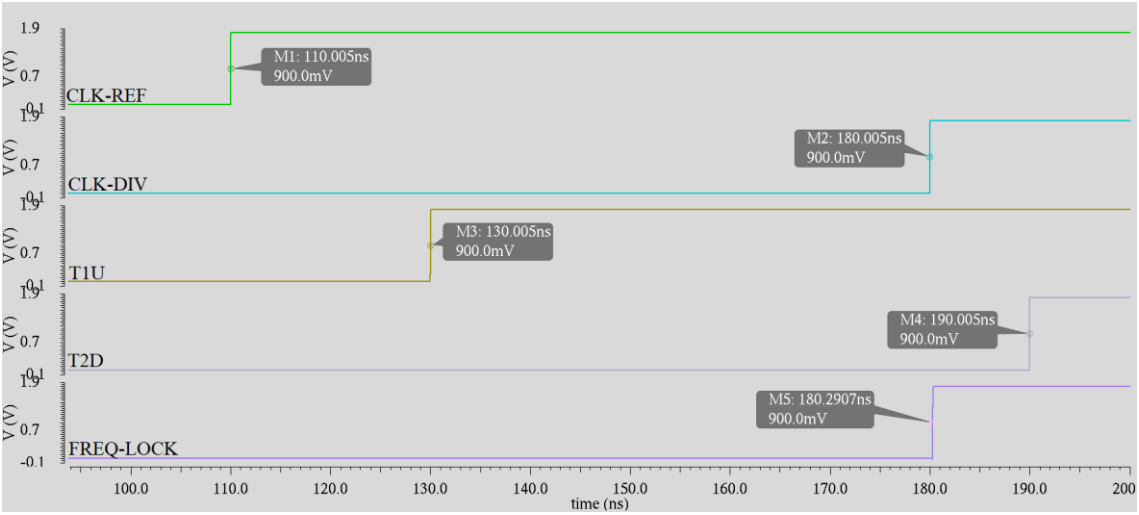

Figure 3.11: Example output for the Frequency Lock module.

When the reference clock comes at 110 ns, T1U is transferred to the output of the first register. Also, at the rising edge of the divider clock at 180 ns, the output of the second register becomes T2D. Finally, after NOR operation "FREQ-LOCK" signal is obtained. Before each phase error evaluation, the frequency lock is reset to "0", and after the evaluation is finalized, it is set to "1" again. In a feedback loop of PLL, frequency lock continuously toggles between "0" and "1", and after frequencies are aligned, it becomes 1 and preserves its state.

3.9. Error Controller

Error correction (controller) block uses 3 registers to catch any synchronization error during the latching process or creation of a delayed version of the loop clock. The error flag that is generated from this module is used as a conditioning primer inside the Hamming Distance module. In other words, this error signal is a significant parameter to regulate the fine error. Error Correction module was designed for both Reference and Divider Clocks to obtain different error flags and the schematics are given in **Figure 3.12**.

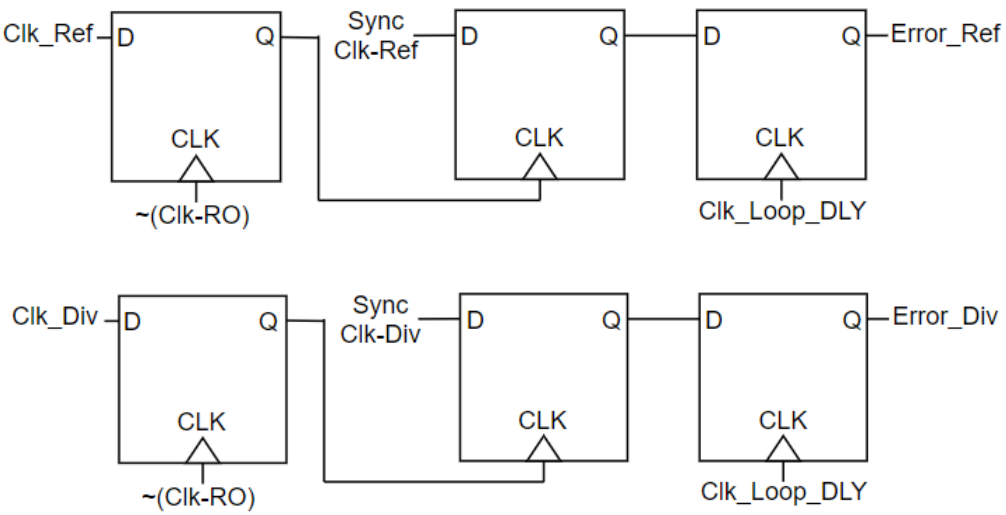

Figure 3.12: Block diagram of the Error Controller modules.

~Clk-RO is the inverted version of the 0^{th} phase of the ring oscillator and as was mentioned before, the initial phase of the ring oscillator was used as a base reference for both hamming distance, synchronization, and counter blocks.

In addition to these blocks, the proposed time to digital converter uses latches for synchronization of the incoming clocks with the initial phase of the Ring Oscillator. Additionally, a buffer was utilized to obtain a 1 ns delayed version of the Loop Clock and an inverter was applied to get Enable signal for initiation of oscillation in the Ring Oscillator. The block diagram of the top module is presented in **Figure 3.1**, at the beginning of Chapter 3.

CHAPTER 4

4. RESULTS AND DISCUSSION

Two different test types were run to observe any error in the design of the proposed time-to-digital converter, which is the Functional and Periodic tests. Functional tests were done to examine specific conditions and to observe the behavior of transitions between each stage. On the other hand, periodic tests demonstrate the response of the TDC phase error for continuously increasing or decreasing phase difference of incoming signals. Functional tests show the response of the system for ideal cases that TDC can achieve the final phase error easily. In other words, a single time difference is applied for a specific time window and TDC keeps that phase error until the end of the simulation. However, periodic tests include dynamic measurement of phase error. This procedure is repeated for multiple cycles to observe and sure about the stability of the design. All details for each measurement technique are explained in the next steps.

4.1. Functional Test Results

As it was mentioned before, functional tests were run to evaluate each scenario that can affect the overall response of the TDC. For instance, the system should give opposite signs when the order of the incoming signal is changed. In other words, if the reference signal leads the feedback, the phase error should be positive, but if, the reference falls behind the feedback then the output signal should be negative. When there is no signal or in reset condition, the result should be 0. However, the phase error of the previous measurement needs to be kept until a new measurement starts.

To evaluate the success of the measurement, fine and coarse distances for both incoming signals were plotted. In addition to them, the ring oscillator's propagation delay was saved, and reference-feedback signals and the final phase error were plotted. After plotting, each analog signal is converted to its digital equivalent to facilitate the

calculation. After all plotting processes, the real propagation delay and the simulation results were compared to measure the experimental phase error and mismatch. Before going into detailed explanations and results, the propagation delay between phases of the ring oscillator should be explained. The difference between phases is important because it directly determines the resolution of the TDC.

Figure 4.1 shows the 14th and 16th phases of the ring oscillator. Oscillation starts when the reset signal is removed from the system at 100 n.

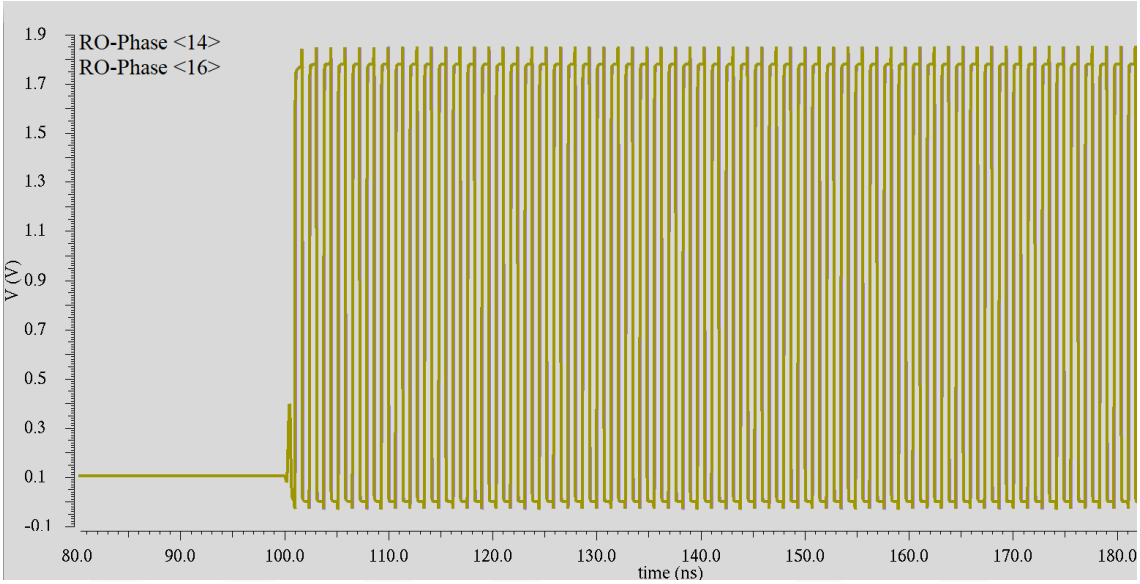

Figure 4.1: 14th and 16th phases of the ring oscillator.

Figure 4.2 presents zoomed version of the propagation delay between the 14th and 16th phases of the ring oscillator. Actual TDC resolution is half of this delay because the 15th phase is in the middle of them, but its sign is negative. In other words, while 14th and 16th phases are rising, it falls from 1.8 V to 0 V.

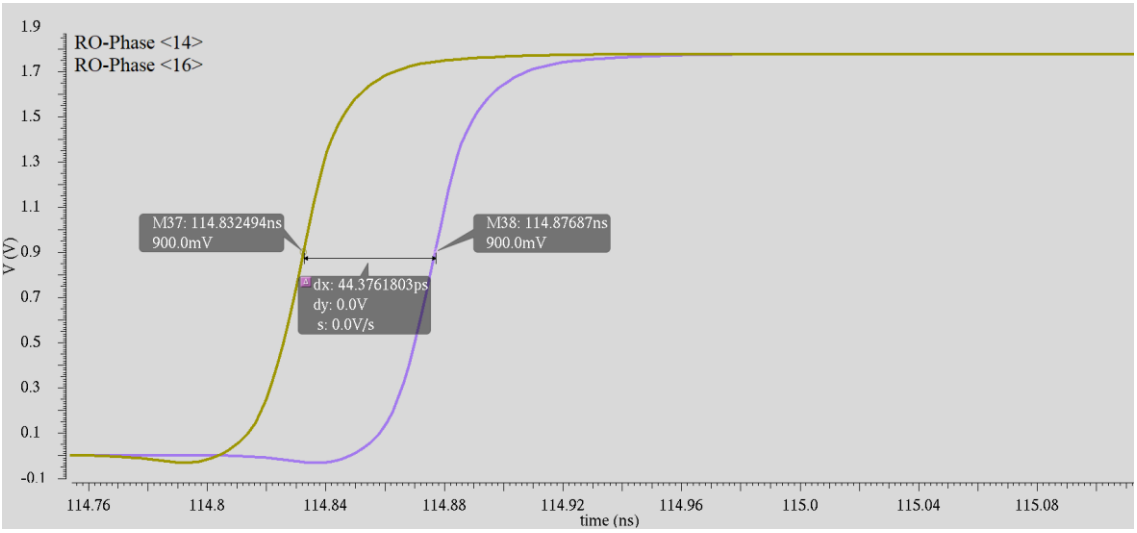

Figure 4.2: Propagation delay between phases.

The time difference between the middle points of those signals is 44.37 ps and as it was explained above, this corresponds to a TDC resolution of 22.18 ps.

4.1.1. 50 ns time difference between Reference and Feedback clocks

Figure 4.3 demonstrates the measurement of the TDC phase error when the time difference between the feedback and the reference clocks are set to 50 ns. The first signal that enters the TDC at 110 ns is the reference signal, and the corresponding counter output is 6. Besides, its fine distance to the 0^{th} phase of the ring oscillator is 44.

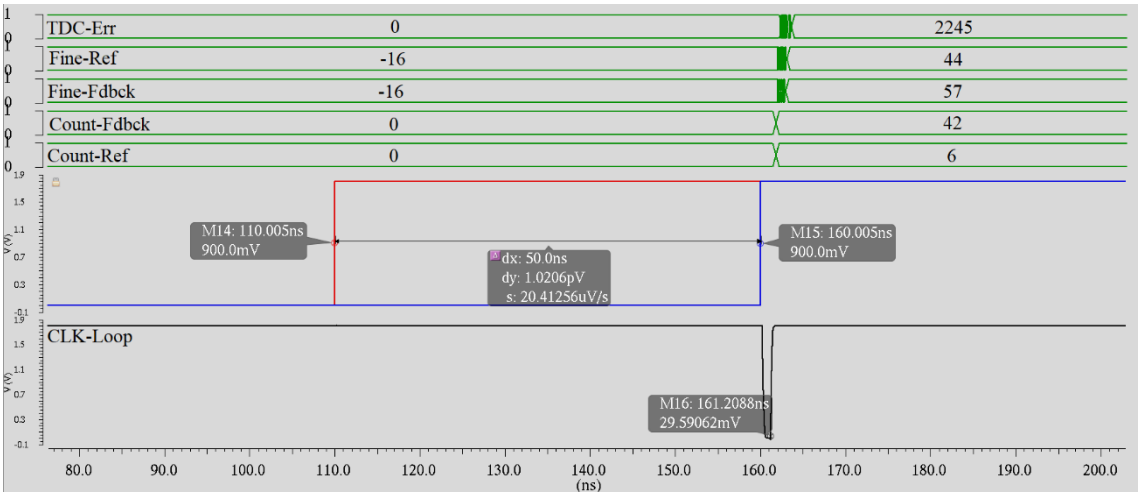

Figure 4.3: TDC phase error measurement for 50 ns time difference.

The second incoming signal is the Feedback, and it arrives at 160 n. The result of the hamming distance block for the feedback signal is 57 and its coarse counter value is 42. After both signals arrive, the clock loop signal is generated in the phase-frequency

detector block and at the rising edge of this signal, the phase error calculation process starts.

$$Fine_{Dif} = Fine_{Fdbck} - Fine_{Ref} \quad \textbf{(4.1)}$$

$$Coarse_{Dif} = Coarse_{Fdbck} - Coarse_{Ref} \quad \textbf{(4.2)}$$

$$TDC_{Err} = \left(62 \times Coarse_{Dif}\right) + Fine_{Dif} \quad \textbf{(4.3)}$$

Equation **4.1**, **4.2** and **4.3** is utilized for the example above. The fine difference is obtained as 13, and the difference between the counter outputs for the incoming signals is 36. However, after the multiplication of the coarse difference with 62 and elongation of the fine difference, the total TDC phase error was calculated as 2245 inside the Manual Transformation block. Furthermore, the ratio between the applied time difference and the calculated phase error should be the same, and equal to the propagation delay of the ring oscillator for all measurements. Propagation delay for each measurement can be obtained via equation **4.4** and it is used to understand the amount of error in the process.

$$Propagation\ Delay = \frac{Time_{Dif}}{TDC_{Err}} \quad \textbf{(4.4)}$$

50 ns time difference results in a 2245-unit phase difference. The corresponding unit step for this measurement was obtained 22.26 ps as explained above. When the designed propagation delay, which is 22.18 ps, and the measured delay were compared, the values match each other with a slight mismatch.

4.1.2. -50 ns time difference between Reference and Feedback clocks

The other functional test that should be run to examine the functionality of the design is the cross-order clock test. In this test setup, the feedback signal arrives earlier compared to the reference signal. To evaluate the success of the measurement, the same time difference was calculated. As it can be seen from **Figure 4.4**, the feedback signal is applied at 110 ns and the reference signal comes at 160 ns.

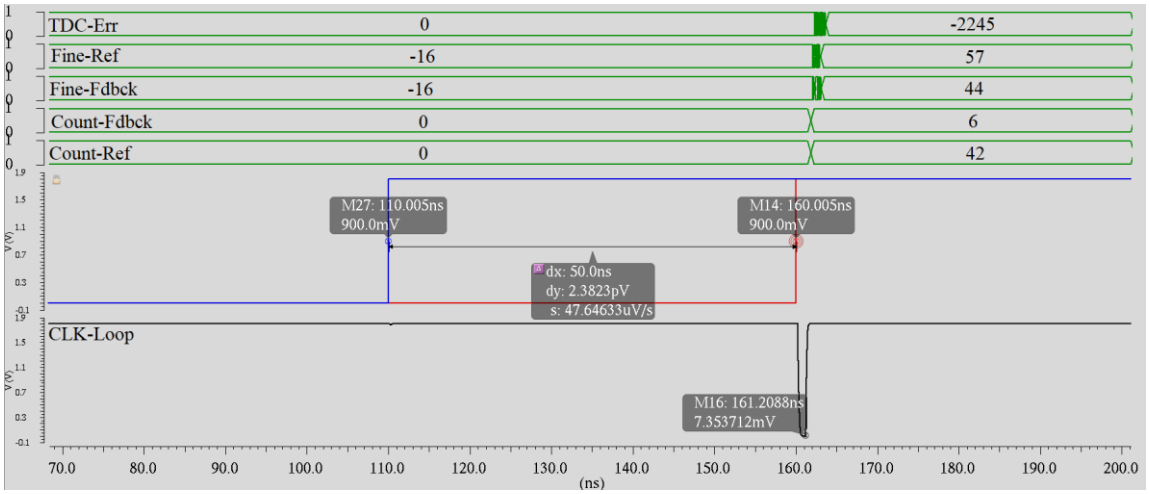

Figure 4.4: TDC phase error measurement for -50 ns time difference.

In this configuration, the time difference between these signals becomes -50 ns, and corresponding counter values and fine results have changed. In other words, the counter result for the reference clock is 42, which is larger than the counter result of the feedback signal. The coarse difference is now – 36, and the difference between their fine results is -13. When all calculations are completed according to equations **4.1**, **4.2**, and **4.3**, the error for the -50 ns time difference is obtained as -2245, which is equal to the negative version of the 50 ns difference. As a result, if the magnitude of the time difference does not change, TDC phase error remains the same except its sign as it is shown in equation **4.5**.

$$|TimeDifference_1| = |TimeDifference_2| \Leftrightarrow |\pm TDC_{Err1}| = |\pm TDC_{Err2}| \quad \textbf{(4.5)}$$

Furthermore, the expected propagation delay of the ring oscillator should not vary between measurements. If the supply voltage and temperature are the same, the system should still use the same propagation delay for measurement, which is equal to 22.18 ps.

4.1.3. 1 ns time difference between Reference and Feedback clocks

The time difference between incoming signals should be decreased step by step to understand any error which can occur during the measurement. For obtaining these errors, the 1 ns time difference was applied to the system and **Figure 4.5** shows the response of the proposed TDC to this specific time interval.

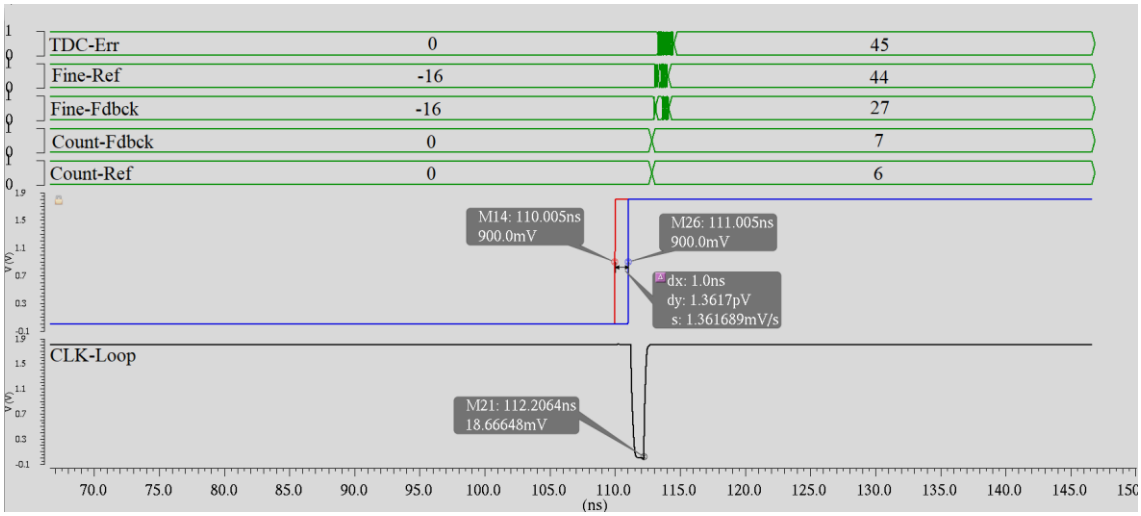

Figure 4.5: TDC phase error measurement for 1 ns time difference.

There is only a difference of "1" between the counter results of the reference and the feedback signals. However, the fine difference is equal to -17 and overall TDC phase error was obtained as 45.

4.1.4. -1 ns time difference between Reference and Feedback clocks

Before going to much smaller time differences, the success of the system for positive and negative time differences should be examined again to observe functionality in smaller time intervals. Like the previous example, the feedback signal was applied before the reference signals to get a negative TDC phase error. **Figure 4.6** demonstrates the signals that contribute to the evaluation of the final result. The feedback signal was applied at 100 n and after 1 ns, the reference signal arrives in the TDC.

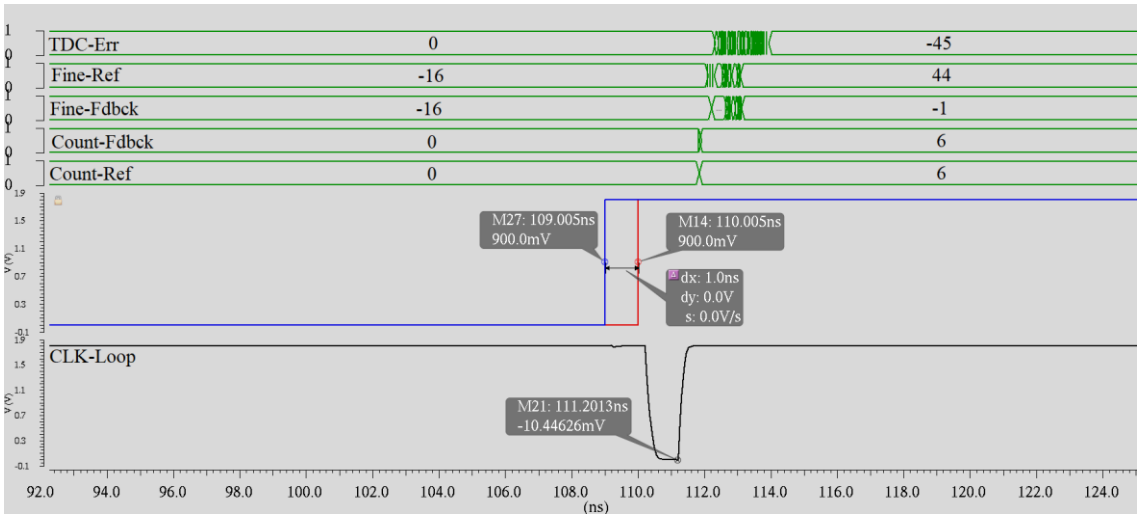

Figure 4.6: TDC phase error measurement for -1 ns time difference.

In this case, results are the same as the expectations and the system gives -45 for -1 ns time difference between signals. On the other hand, internal signals and main contributors are different from the positive equivalence of this example. There is no contribution of counter results for this interval, and this can be seen from coarse difference which is equal to 0. In other words, TDC phase error only depends on the fine difference between clocks. And this phenomenon preserves itself for smaller time differences.

4.1.5. 0.125 ns time difference between Reference and Feedback clocks

The time difference between reference and feedback signal was lowered to 0.125 ns to investigate any miscalculation or mismeasurement of the final phase error. First of all, reference and feedback signals were applied at 110 ns and 110.125 ns, and after that measurement had started when the CLK-Loop signal was triggered. **Figure 4.7** demonstrates significant contributors to the evaluation process.

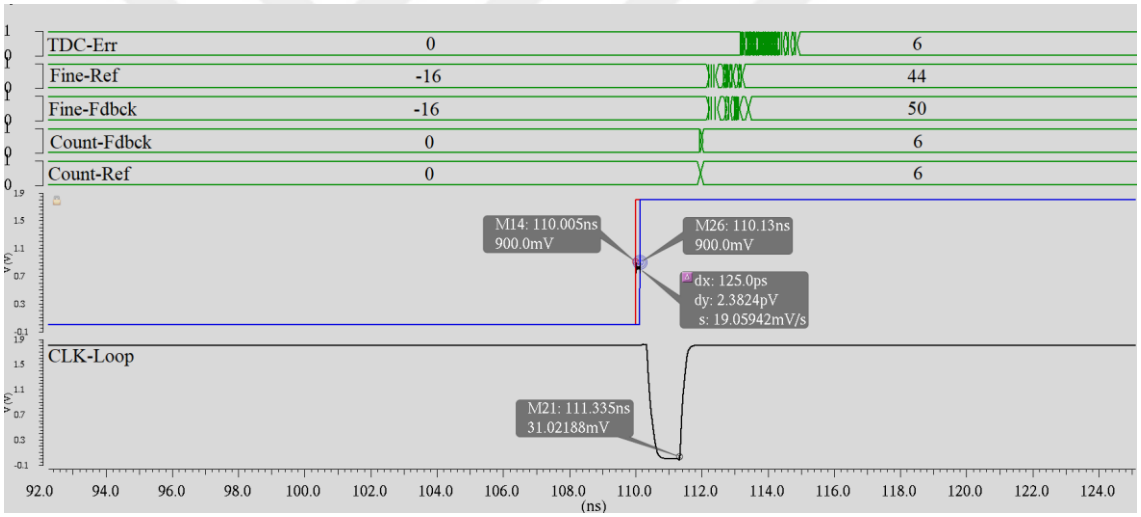

Figure 4.7: TDC phase error measurement for 0.125 ns time difference.

Similar to the 1 ns time difference case, the contribution of the coarse difference is 0, and phase error depends only on the fine difference between signals which is equal to 6. Nevertheless, the propagation delay formula should still hold for small differences, and when it's calculated 20.8 ps propagation delay was obtained. There is a minor difference between this result and the expected propagation delay. The correct phase error reading for the corresponding time difference should be 5.6 but because the 0.125 ns is not an integer multiple of 22.18 ps, so system gives the closest phase error that can represent this time interval digitally which is 6. The integer-multiple phenomenon is not effective in the measurement of bigger time intervals because the contribution of the fine distance is

negligible. In other words, when the time interval is a non-integer multiple of propagation delay, the proposed TDC rounds the error to give as close as possible to the real one.

4.1.6. 0.102 ns time difference between Reference and Feedback clocks

Linearity is one of the most significant parameters that define the performance and quality of the TDC. The amount of nonlinearity is determined from the transfer curve of the relation between the time difference and the digital output. However, another method that can be employed to understand linearity is increasing or decreasing the time difference by unit steps and observing the response at the output. To investigate this analogy, the 0.125 ns time difference was decreased by the amount of resolution that is equal to 22.18 ps and then used as the time difference between the reference and the feedback signals.

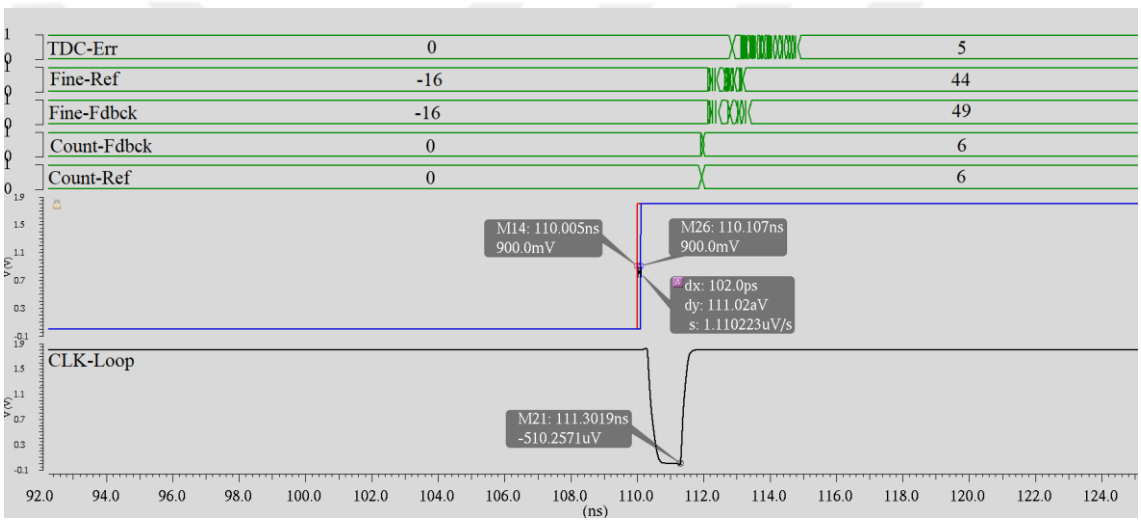

Figure 4.8: TDC phase error measurement for 0.102 ns time difference.

TDC phase error can be calculated from only the fine difference between signals and as it can be seen from **Figure 4.8**, it is equal to 5. With respect to the linearity property of TDC, it can be said that if there is a unit variation in time difference, there should be also a unit difference in TDC error. In other words, when the time difference is decreased in an amount that is the same as resolution, TDC error decreases by “1”.

Further analysis of the functional tests was performed without graphing. **Table 4.1** shows the TDC phase errors and significant signals for randomly selected time differences. For each measurement, the mismatch between TDC readings and the real-time differences was investigated.

Table 4.1: Functional test results.

Time Dif. (ns)	Count Ref	Count Fdbck	Coarse Dif.	Fine Ref	Fine Fdbck	Fine Dif.	Measured TDC Phase Error	Calc. Time Dif. (ns)	Mismatch (ps)
60	6	50	44	44	11	-33	2695	59.775	225
75	6	61	55	44	2	-42	3368	74.702	298
16	5	16	11	17	53	36	718	15.925	74.8
-16	21	10	-11	57	21	-36	-718	-15.925	74.8
4	6	9	3	44	38	-6	180	3.9924	7.6
2	13	15	2	59	25	-34	90	1.9962	3.8
19.2	3	17	14	5	-2	-7	861	19.096	103.02
45	3	35	32	5	43	38	2022	44.847	152.04
0.8	13	14	1	59	33	-26	36	0.79848	1.52
-80	68	10	-58	18	21	3	-3593	-79.693	307
21	3	18	15	5	19	14	944	20.938	62.08
0.24	12	12	0	31	42	11	11	0.24398	-3.98
0.5	10	10	0	21	43	22	22	0.48796	12.4
-0.3	10	10	0	34	21	-13	-13	-0.28834	11.26
47	7	41	34	47	50	3	2111	46.82198	178.02
0.15	6	6	0	44	51	7	7	0.15526	-5.26
0.172	6	6	0	44	58	8	8	0.17744	-5.44

Results in **Table 4.1** show that the proposed TDC works successfully for different input signals of short or long-time differences. Actually, there are three significant indicators that show TDC works properly, and they were expressed by using examples that are presented in **Table 4.1**.

The first one is the sign of the result. As it was mentioned, if the reference clock leads the feedback clock, in other words, if the reference clock comes before the feedback signal, the output of the TDC should be positive. On the other hand, if the feedback signal comes before reference, then the sign of the result should be negative. For example, 16 ns time difference and -16 ns, results have the same magnitude, but their sign is different.

The second indicator is linearity and the sensitivity of the TDC for small values. The overall calculation mechanism should be the same for not only large time intervals but also small-time windows. Here the most important point is; when the time difference between inputs are small, coarse distance losses its effects on the final result and fine distance becomes the main contributor to the TDC output. Moreover, when the time window is increased by an amount of resolution, phase error should increase by 1. This

phenomenon can be observed in 0.15 ns, and 0.172 ns examples. As is shown in **Table 4.1**, their coarse difference is zero, and it has no effects on the final result. Also, the difference between their final phase errors is 1 which is unitary.

The last and the most significant indicator of success is the equivalence of the calculated time difference and real-time difference. The calculated time difference is obtained when the TDC phase error is multiplied by the designed propagation delay which is 22.18 ps. Small-time differences have smaller mismatches than the larger ones. This phenomenon is directly related to the INL and DNL of the converters. For example, when 0.8 and 0.24 nanosecond time differences were investigated, both of them can be digitized with a couple of picosecond mismatches which are directly negligible and no significant effects on the functionality. On the other hand, larger time intervals like 60 ns or 80 ns ones tend to have more mismatches than smaller ones. As it was mentioned before, this is the result of an INL, which is integrated nonlinearity. Mismatches accumulate and grow when the phase difference between incoming signals increases. However, in the feedback loop system of PLL, large time differences are compensated during coarse tuning and after frequency scaling in the divider, the time difference between signals decreases. During the fine-tuning stage of the PLL, TDC deals with very small time differences which have also very small mismatches. In other words, large time intervals were eliminated in coarse tuning and their mismatches become negligible.

As a result, functionality analysis of the proposed TDC is completed by using this method, and testing was continued with repetitive periodic measurements.

4.2. Periodic Test Results

The second type of simulation that shows the success of the error measurement is the periodic test. The first step of this process is adjusting the frequency of the input signals. Periods of the incoming signals should be chosen as close as possible to observe even the smallest errors. In each iteration, which means in each measurement, the amount of the decrement or increment should be equal. In other words, the difference between the successive errors should be equal among all the steps. Equation **4.6** shows the analogy behind the success criteria of periodic tests.

$$(|TDC_{Err}(n+1)| - |TDC_{Err}(n)|) = (|TDC_{Err}(n+2)| - |TDC_{Err}(n+1)|) \quad \textbf{(4.6)}$$

For example, if "n" is equal to 32, the difference between 32nd sample and the 33rd sample should be equal to the time difference between 33rd and 34th samples. To investigate this phenomenon with real signals, 4 different test setups were constructed. Periods of the reference and feedback signals were set to 50-49 ns, 50-47 ns, 50-43 ns, and periods with decimal numbers, to test various cases. However, the common property of these signal pairs is they do not have a common divisor. In other words, phases of the signals cannot align because of beat frequency, they only catch each other when convergence is completed.

4.2.1. Periodic Test results for 50-49 ns input signals

The period of the reference signal is set to 49 ns and the feedback signal to 50 ns and applied to the inputs of the TDC. **Figure 4.9** shows the digital TDC phase errors for repetitive measurement.

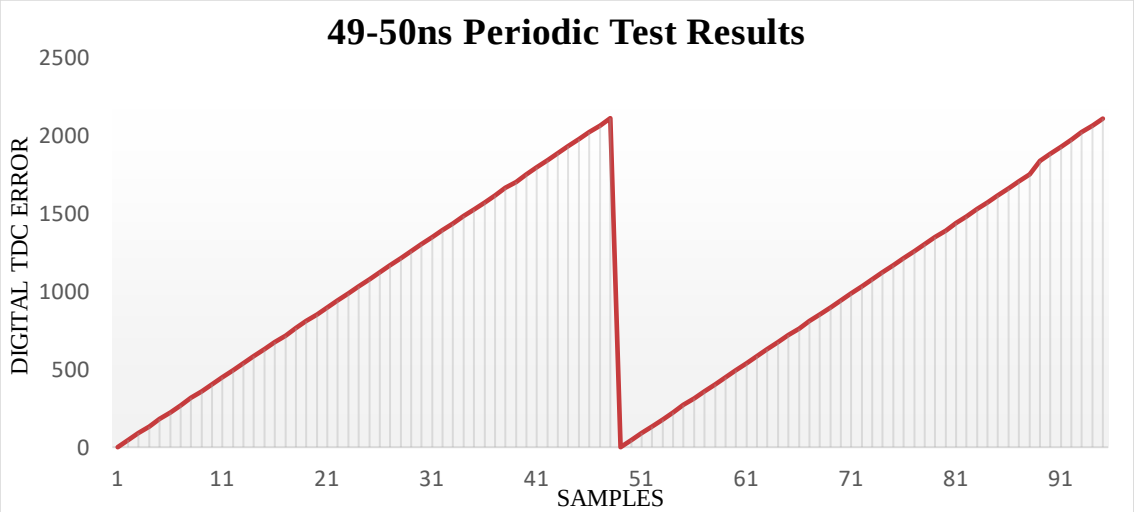

Figure 4.9: Periodic test results for signals with 49-50 ns periods.

The most significant parameter that shows the success of the measurement is linearity and **Figure 4.9** shows that the proposed TDC has almost equal steps between each measurement. The phase difference between those signals continuously increases because they move away from each other in every period. At the middle of the graph (at 2.57µs), two signals catch each other, and their phases align automatically. In those cases, TDC phase error starts to rise from "0" again. In other words, after the convergence, the second deviation starts, and phase error increases again. However, **Figure 4.10** is the zoomed version of the phase error for a periodic measurement.

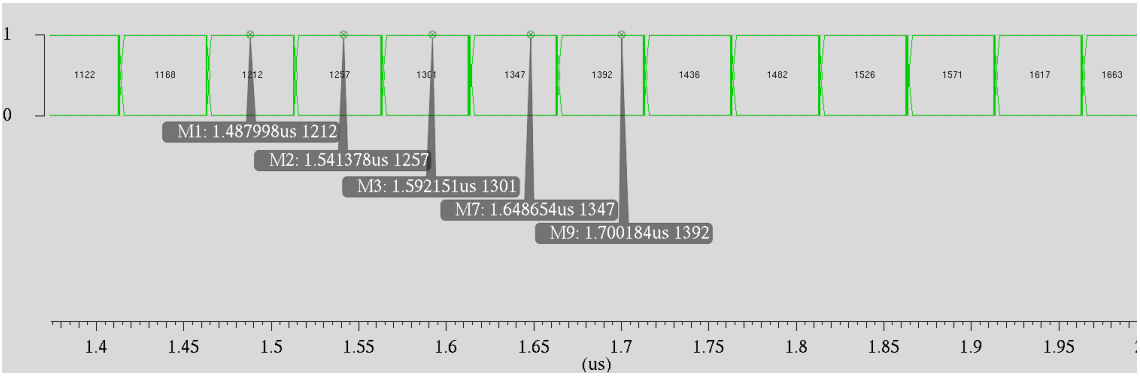

Figure 4.10: Zoomed version of the 49-50 ns periodic measurement.

The most significant part is maintaining the stability of the differences between two successive steps. In other words, the rate of divergence between those measurements should be equal as was mentioned. In **Figure 4.10**, the measurement axis was zoomed to observe digital phase errors easily and 5 different probes were employed to observe randomly selected five successive measurements. The difference between the first and the second marker is 45, and the difference between the third and the second one is 44. Instead of checking these differences one-by-one, a calculator script is employed to evaluate the amount of variation.

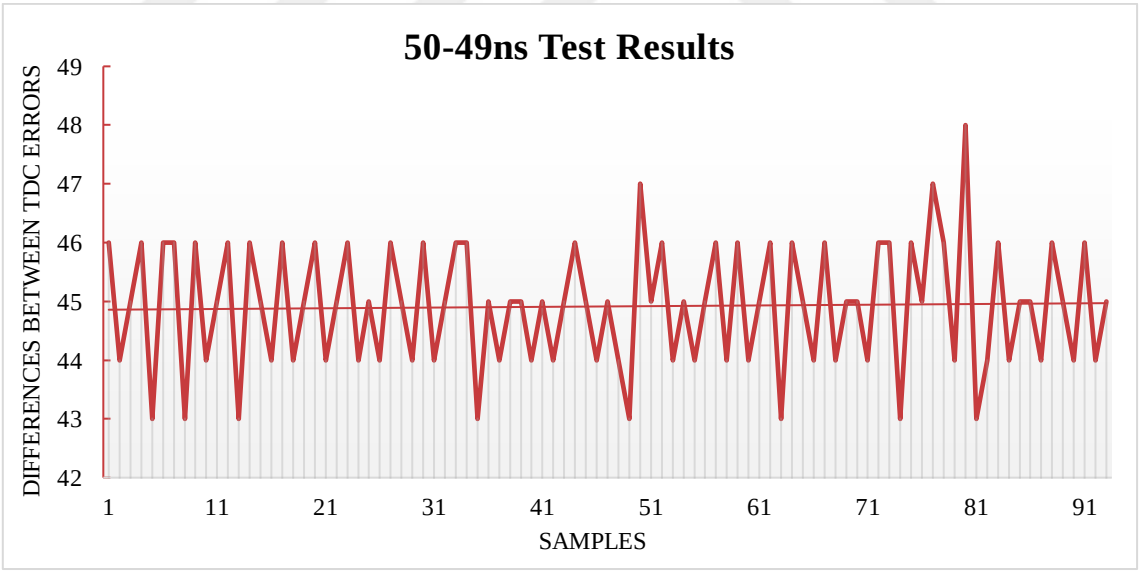

Figure 4.11: Differences between each successive step for signals with a 50-49 ns period.

Figure 4.11 shows the results for the difference between phase errors of each sample, and the average value was obtained as 45. The largest variation from the average phase error (45) is equal to +3 and the average variation is ±1. This phenomenon shows that the digitization mechanism is working without any fine measurement error.

As it was mentioned in the Method part, fine measurement depends on the utilization of

the ring oscillator's phases for input signals. However, using the wrong phases can lead mismatch between successive TDC measurements. The error correction block is employed to fix the wrong phase transition during fine distance calculation. Actually, it checks the synchronization of the input signals and creates an error flag that regulates conditions in the hamming distance block. This regularization changes the sign of the fine difference of corresponding input and prevents the miscalculation of error. If both inputs have erroneous phases, which is 31 bits, the fine difference can be obtained with a ±62 unit mismatch than the original one. In other words, without using the error correction module, the difference between each successive measurement can vary up to ±62, which is not acceptable.

4.2.2. Periodic Test results for 50-47 ns input signals

To examine another signal pair, the period of the reference signal is set to 47 ns, and feedback was applied with the 50 ns period. The measurements are shown in **Figure 4.12**.

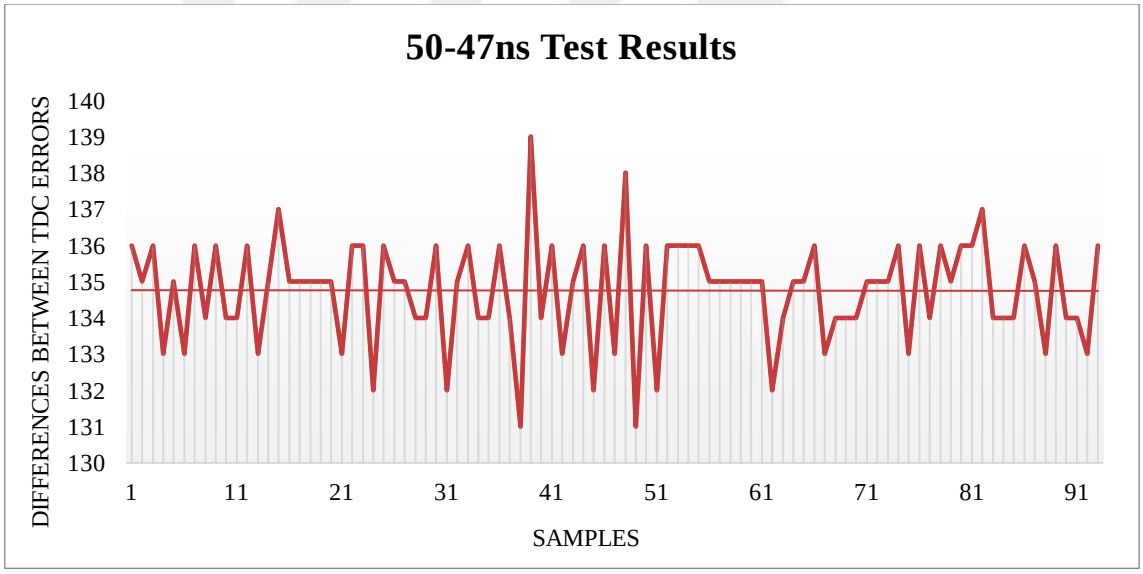

Figure 4.12: Differences between each successive step for signals with a 50-47 ns period.

As expected, differences between measurements are obtained with only small variations. However, the effects of those small variations are negligible, and a correct average can be achieved in the PLL to function correctly. For this case, the average phase error between successive steps is 135, and its maximum variation is ±4.

4.2.3. Periodic Test results for 50-43 ns input signals

Another test that can be implemented to observe the convergence faster than the previous test is using the 50-43 ns signal pair. In this test, phases of reference and feedback signals are aligned much faster and TDC result changes with larger steps. Zoomed version of the test results in **Figure 4.13** demonstrates two distinct phenomena that were mentioned.

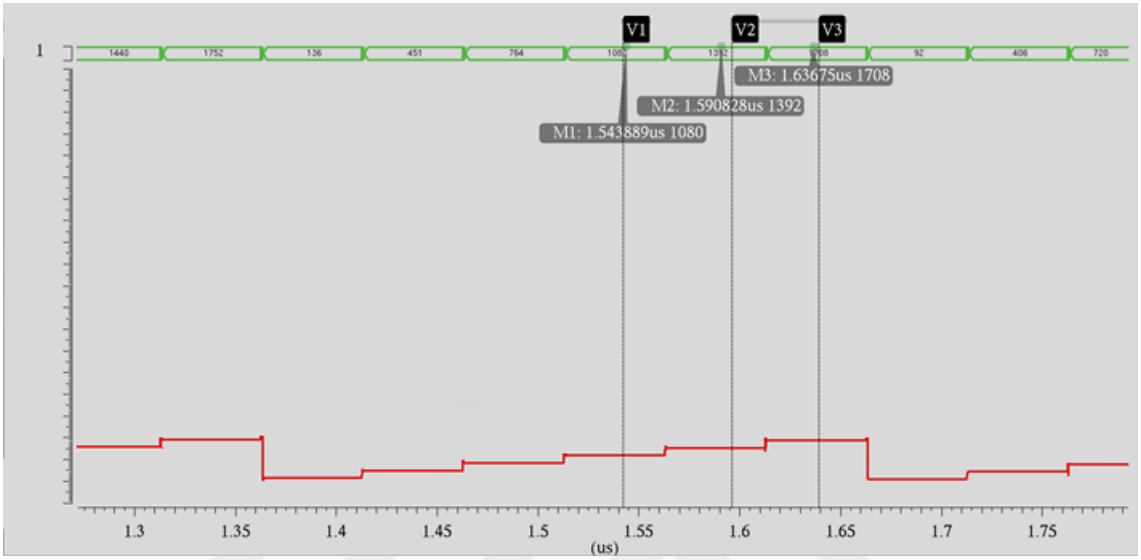

Figure 4.13: Zoomed version of the 43-50 ns periodic measurement.

Signals align automatically at 1.365 µs and 1.665 µs which shows the speed of convergence, and it is significantly faster than the 50-49 ns pair.

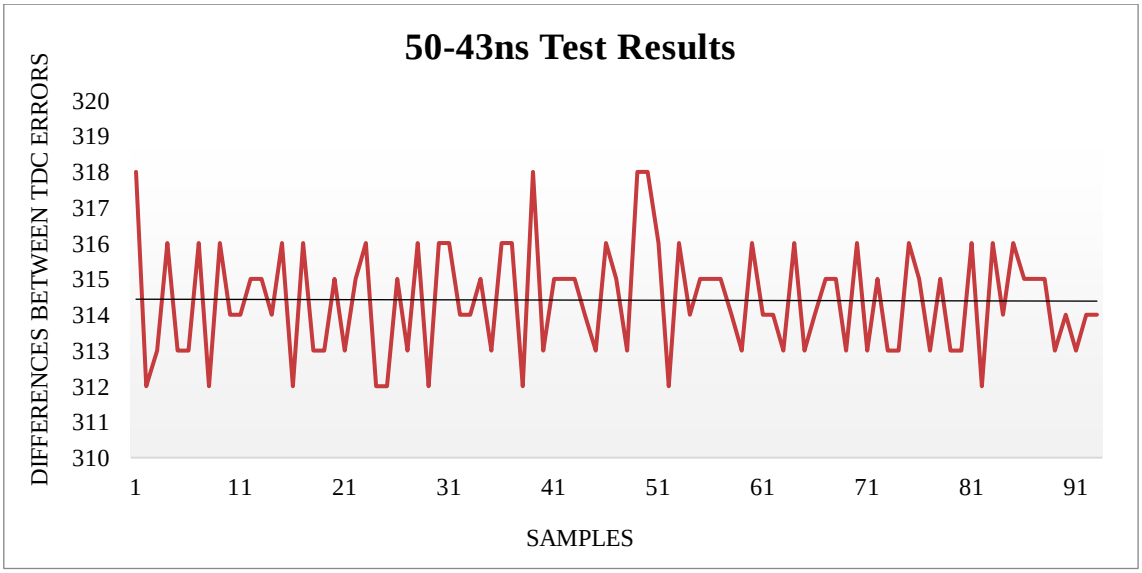

Figure 4.14: Differences between each successive step for signals with a 50-43 ns period.

The average difference between measurements is 314 as seen in **Figure 4.14**, which is larger than the previous examples. However, the system is consistent, and results were

obtained with a maximum variance of 4.

As a result of these measurements, it can be said that the response of the proposed TDC is valid and correct, during the repetitive measurement of the phase error. The difference between the steps is consistent for each iteration and thanks to the error controller module of the TDC, sudden jumps or inconsistent differences are prevented in the final result. As explained before, the "error controller" module works with hamming distance module to check the corresponding phases for each input signal. If there is an error while catching those phases, they regulate the fine difference to reduce the amount of error at the final output of TDC. After periodic tests, the proposed TDC was simulated and verified across PVT.

4.3. PVT (Supply Voltage and Temperature Dependency)

The proposed TDC is expected to operate between -200 ^{o}C and 85 ^{o}C degrees without any malfunctioning after manufacturing. In addition to these different temperatures, supply voltages were varied ±10% to observe any error during the calculation of TDC phase error. Furthermore, corner simulations with temperature and supply voltage combinations were run to ensure that the design works smoothly under all conditions. **Table 4.2** shows the dependency of the TDC readings on voltage-temperature variations for a typical corner.

Table 4.2: Variations in the phase errors for different voltages and temperatures.

Time Difference (ns)	**Normal (1.8V 27^{o}C)**	**-40^{o}C**	**-200^{o}C**	**85^{o}C**	**1.62 V**	**1.98 V**
0.8	36	40	53	33	33	38
3	135	148	201	125	124	145
-1	-45	-49	-66	-41	-41	-47
50	2245	2459	3356	2085	2062	2408
60	2695	2951	4029	2502	2475	2890
70	3143	3443	4701	2919	2888	3372
80	3593	3935	5372	3336	3299	3854
50.5	2268	2484	3391	2106	2084	2432
51	2291	2509	3425	2127	2104	2456
60.03	2696	2952	4031	2503	2576	2891
70.5	3166	3468	4734	2939	2908	3394

Transistors operate faster in low temperatures and this phenomenon can be observed from the TDC phase errors in **Table 4.2**. When the temperature is lowered, the frequency of the ring oscillator increases, and the propagation delay between each phase decreases. The resolution of TDC takes the advantage of this speed boost, in other words, the time difference between the input signals can be calculated finer in low temperatures than the room temperature. On the other hand, the opposite of this phenomenon is valid for high temperatures. If the operating temperature increases, transistors slow down, and the delay between the inverters increases. Moreover, the resolution of the TDC drops and same time differences are presented with smaller errors. Also, when the supply voltage increases, the propagation delay between inverters decreases, and the resolution of the TDC increases. Further analysis of the temperature and voltage dependency of the final result is completed by combining different conditions and **Table 4.3** shows the results for this analysis.

Table 4.3: Effects of the combination of different voltages and temperatures.

Time Difference (ns)	1.62V -40°C	1.62V -200°C	1.62V 85°C	1.98V -40°C	1.98V -200°C	1.98V 85°C
0.8	36	50	30	43	56	36
3	136	189	114	157	211	133
-1	-45	-63	-38	-51	-70	-45
50	2270	3151	1909	2619	3509	2249
60	2724	3781	2291	3143	4212	2699
70	3179	4414	2673	3665	4916	3148
80	3633	5044	3054	4191	5618	3599
50.5	2293	3184	1928	2644	3546	2272
51	2316	3216	1947	2672	3581	2294
60.03	2725	3783	2291	3144	4214	2700
70.5	3202	4444	2692	3693	4951	3171

When the temperature decreases and supply voltage increases, transistors work at their maximum speed and this behavior maximizes the resolution of the TDC. Moreover, the system represents the same time difference with larger digital error. On the other hand, low supply voltages and high temperatures affect the system negatively in terms of speed and resolution. The worst condition in terms of speed can be described as 1.62 V at 85 °C and the best one is 1.98 V supply at -200 °C. However, when the results were compared in each group of conditions, in other words, the effective propagation delay for each

column is obtained as equal for all of the time differences. In essence, measurements are consistent and there are no erroneous calculations. Furthermore, the difference between the real and the calculated time differences was investigated and the amount of mismatch was obtained without any abnormality. Actually, the real reason behind these variations is the increasing or decreasing operating frequency of the ring oscillator.

Table 4.4 demonstrates the direct relationship between temperature & voltage variations and the operation boundaries of the ring oscillator.

Table 4.4: Temperature and Voltage dependency of Ring Oscillator specs.

Voltage (V)	Temperature (°C)	Ro_Freq (MHz)	Ro_Period (ns)	Propagation Delay (ps)
1.8	27	727.2	1.375	22.18
1.8	-40	799.4	1.251	20.33
1.8	-200	1079	0.927	14.89
1.8	85	672.5	1.4869	23.98
1.62	27	665.1	1.5038	24.24
1.62	-40	732.6	1.365	22.02
1.62	-200	1016.3	0.984	15.86
1.62	85	617.3	1.62	26.19
1.98	27	776.9	1.2872	20.76
1.98	-40	844.9	1.1835	19.09
1.98	-200	1132.5	0.883	14.24
1.98	85	729.9	1.37	22.23

When the temperature and the supply voltage increase, the operating frequency of the ring oscillator increases, and the propagation delay between inverters decreases. In other words, our fine reference, becomes smaller and finer. In the fastest case, resolution becomes 14.24 ps. On the other hand, at higher temperatures resolution becomes worse and the fine measurement capability of the device decreases up to 26.19 ps. In addition to all conditions above, the worst, the best, and the nominal values are examined with process corners. To realize this simulation, technology files of the transistors were changed in ADEL and worst power - worst speed scenarios examined across temperature and supply voltage variations. **Table 4.5** and **Table 4.6** show the measurement of different time intervals and ring oscillator's operation specs across all conditions.

Table 4.5: Error measurements in different corners.

Delay (ns)	Normal Typical (1.8 V 27ºC)	Worst Speed Slow-Slow (1.62 V, 85ºC)	Intermediate Fast-Fast (1.98 V, -40ºC)	Worst Power Fast-Fast (1.98 V, -200ºC)
0.8	36	25	50	57
3	135	95	182	235
50	2245	1586	3034	3919
60	2695	1903	3641	4701
70	3143	2220	4246	5486
80	3593	2536	4855	6270
50.5	2268	1602	3064	3958
51	2291	1617	3095	3999
60.03	2696	1903	3642	4703
70.5	3166	2236	4278	5524

Table 4.6: Behaviors of the Ring Oscillator in different corners.

Voltage (V)	Temperature (ºC)	Corner	Ro_Freq (MHz)	Ro_Period (ns)	Propagation Delay (ps)
1.8	27	Typical	727.2	1.375	22.18
1.98	-40	Fast-Fast	976.6	1.024	16.48
1.98	-200	Fast-Fast	1259	0.794	12.76
1.62	85	Slow-Slow	512.03	1.953	31.53

When the fastest operational condition is employed with devices that can operate faster than normal transistors, the speed of the oscillation increases up to 1.26 GHz. In other words, the resolution of the TDC is maximized in the fast-fast corner and it is equal to 12.76 ps. On the other hand, the ring oscillator consumes more current to oscillate at higher frequencies. In other words, the process affects the power consumption of the ring oscillator. Besides, when transistor model that operates slower than a typical one is employed with low supply voltage at higher temperatures, the resolution of the TDC becomes 31.53 ps which is the worst-speed scenario because the current consumption of the ring oscillator decreases when the supply voltage decreases. Low power supply and high temperature also negatively effects the frequency of the oscillator. In summary, power consumption and frequency increase when the temperature decreases and power supply voltage increases.

As a result, even if the proposed TDC was tested at worst-case corners, no errors or any malfunction were obtained in any measurement.

4.4. Layouts

The proposed TDC was initially designed with Verilog. Once the design was tested with the Verilog compiler and successfully pass from every single test, the RTL synthesis tool of Cadence was employed to realize the circuit. To achieve the ultimate performance in the lowest area, a pre-defined standard cell library that includes logic gates with different sizes was utilized. The first step of the synthesis is abstracting the power and the specs of the cells in the standard cell library. Additionally, pre-defined terminal scripts were prepared to facilitate the process of placing and routing.

On the other hand, for each sub-module, there are different time specifications to achieve correct clock timing and delay requirement. Synopsys Design Constraint file contains all that information to adjust the design process. Capacitance and period values for the artificially inserted input clocks are the most significant parameters for the synthesis. For instance, the output schematics of the synthesis tool for the fast and slow frequency counters are different from each other, and to achieve the correct design, time specs should be given to the tool precisely. The same phenomenon is valid for the design of every single submodule, and the common input clock period for them is 50 ns which is the same as the period of the clock loop signal. However, there are some exceptions like the 8-bit counter, which utilizes the period of ring oscillator as an input clock period during synthesis.

When RC synthesis of the Verilog codes is completed, new gate-level Verilog codes were obtained. After that point, Place and Route process was started with pre-prepared Tool Command Scripts. The most significant part of the routing process is placing the standard cells most efficiently to consume less area in a microchip. Conveniently, there are very strong optimization techniques that are used by Cadence Encounter. Besides, if any timing violations occur during the process, they are resolved by inserting buffers into high fanout paths. After the place & route process is completed, the final version of the gate level Verilog file, and the design exchange file, which contains information about all layers and vias is obtained. As the last step of the generation of schematic and layout, final versions of the files are imported to a corresponding library.

Even though Cadence Encounter is a strong tool for the synthesis process, some blocks should be designed manually for better optimization. In this thesis, the schematic and layout of multi-input inverters and 31 phases ring oscillator were designed manually. The most significant technique that is used during design is minimizing the wiring between

the transistors in the inverter. Moreover, the length of the wires between each inverter should also be kept short to achieve less delay after the post-layout parasitic extraction process. Furthermore, to adjust and balance the output capacitance of each inverter in the ring oscillator module, buffers were inserted after their outputs.

4.4.1. Layout of the Multi-Input Inverter

The most significant block that directly determines the resolution of the overall TDC is the inverter in **Figure 4.15**. Besides the sizing of the transistors, the layout of the design is also important to reduce the parasitic effects. To ensure this, all transistors and power lines were placed in a most compact way. The length and width of the overall design were also determined based on the optimal placement of all standard cells.

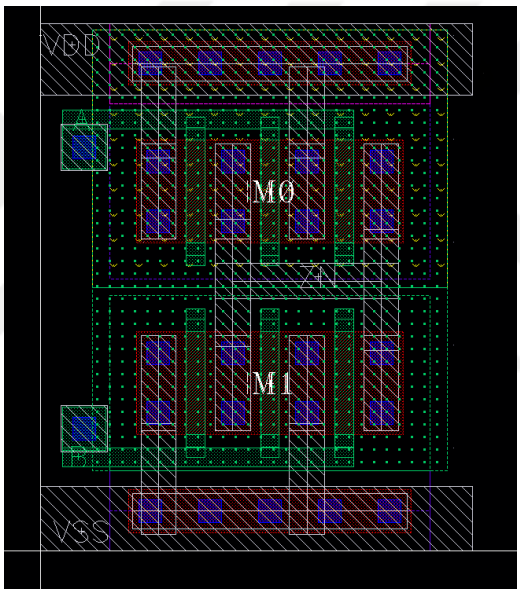

Figure 4.15: Layout of the Multi-input Inverter.

4.4.2. Layout of the Ring Oscillator

Figure 4.16 shows the layout of the 31 phases multi-input ring oscillator. The core part in the middle consists of inverters that are used in the design of the ring oscillator. The outer shell of the design consists of buffers that are placed to prevent unbalanced capacitive load for each phase of the RO. Moreover, the part on the right of the layout is a supply switch that is used for disabling the RO. The current consumption of the ring oscillator is considerably larger than the other modules and to minimize IR drops in the supply line, widths of the VDD and VSS lines are kept as large as possible. The overall length and width of the module are presented in the gate-area report section.

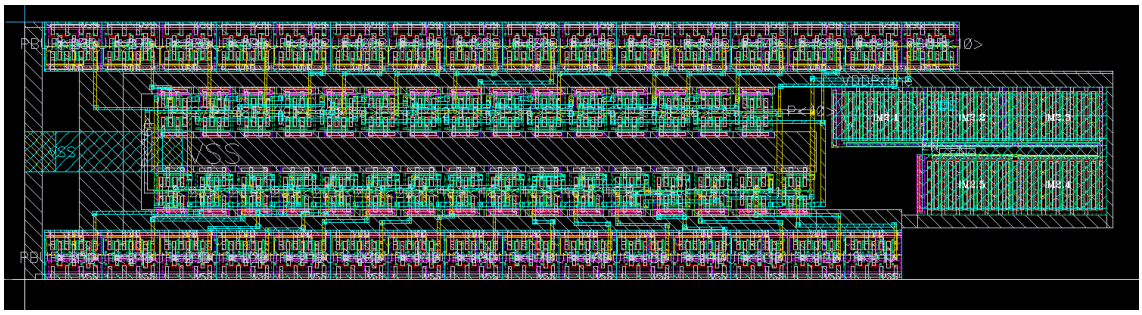

Figure 4.16: Layout of the Ring Oscillator.

4.4.3. Layout of the Frequency Detector

Figure 4.17 shows the layout design of the Frequency lock module, which is synthesized with Encounter first, then modified manually to optimize the area and timing. Detailed information about sizes was included in the gate-area report section.

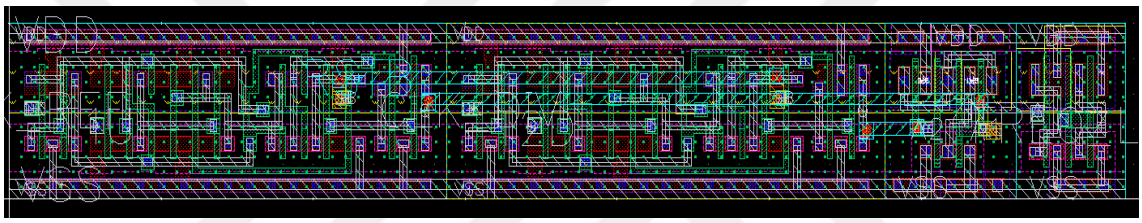

Figure 4.17: Layout of the Frequency Lock module.

4.4.4. Layout of the Phase-Frequency Detector

The most problematic feature of synthesizing gate-level Verilog code with RC and Encounter tools is losing the specific delay values inside the behavioral Verilog models. In order to meet timing to function properly, buffers need to be placed in the correct places that specific delays are required. In other words, synthesized schematic and layout should be manually optimized with some buffers to meet the timing and to realize appropriate function at the circuit level. Due to the reasons above, buffers were added inside the PFD manually to adjust the internal resetting mechanism which was explained in the method part. **Figure 4.18** shows the manually modified phase frequency detector layout, which employs input signals to generate pulses to control the initiation of the measurement in the TDC.

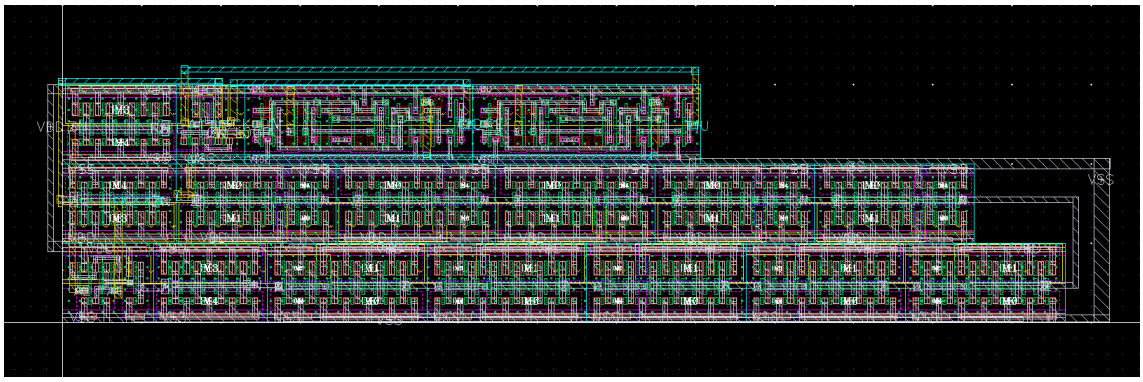

Figure 4.18: Layout of the Phase Frequency Detector.

The largest block in the PFD layout belongs to a buffer which is used to regulate the internal reset mechanism of the phase-frequency detector. Similar to the ring oscillator design, sizes of the VDD and VSS lines are important to adjust the current density but, in this case, instead of increasing the widths in submodule level, all sizes were combined and re-sized in top module design.

4.4.5. Layout of the Digital Modules

All other modules like hamming distance, manual transformation, error correction and, D-flipflop arrays are synthesized without adding any extra instances or gates inside the module. There are two main reasons to generate them directly without any further adjustments. Firstly, since the timing requirements for this block are quite loose and can be met easily with the synthesis operation. Secondly, the power and the precision of Cadence Encounter in terms of optimizing a design offers a much faster and compact solution compared to a manual design. **Figure 4.19** shows the layout for all the digital modules in the proposed TDC.

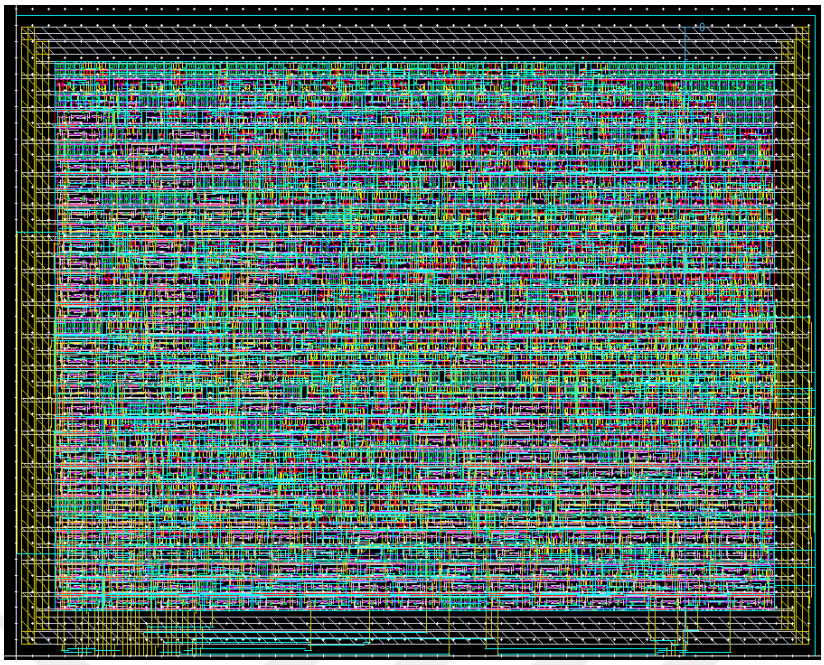

Figure 4.19: Layout of the Digital Module.

The number of lines and width of columns was adjusted concerning floorplan specs of the project and the length of the standard cells. The density of the design was adjusted to % 90 percent and the remaining empty parts are filled via Filler cells.

4.4.6. Layout of the Top Module

To combine the digital modules, phase-frequency detector, frequency lock, and ring oscillator modules, a new layout was constructed manually. The design was optimized for the smallest area with the shortest wiring. In order to minimize the IR drop across them, the minimum width for the power lines was set to 4 µm. Also, the output and input pins of the TDC were placed on different edges for optimal connection distance. In the layout of the submodules, only the first 3 metals were utilized to reserve the rest for top-level routing and connections. All other details about length and width values were presented in the area report sections. **Figure 4.20** shows the layout of the TDC top module.

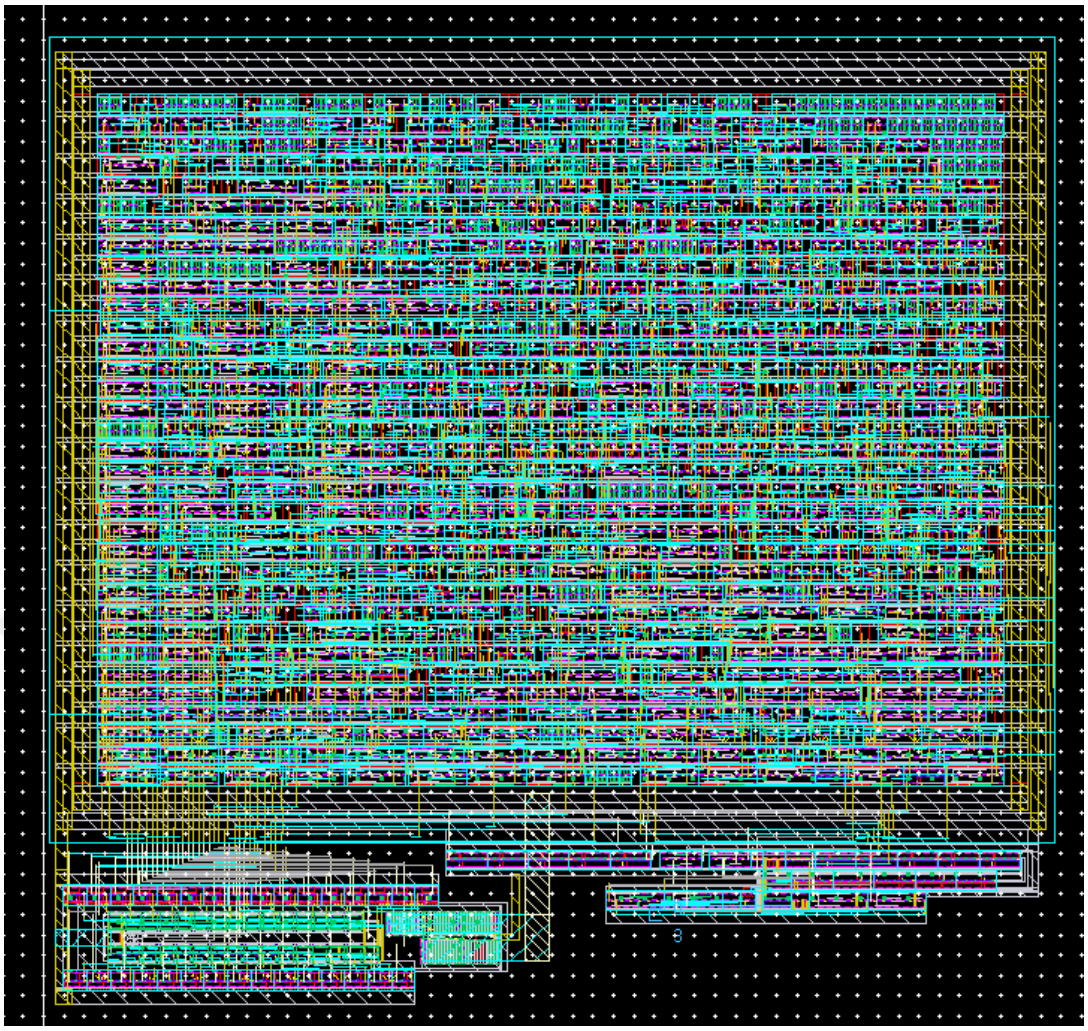

Figure 4.20: Layout of the Top Module.

The main and the most significant part of the design is placed at the core side of power rings. At the lower-left side, the ring oscillator with buffer ring was placed without violating any current density rules. Moreover, PFD, frequency lock, latches, and buffers were grouped first, then combined with other parts at the lower right side of the TOP module.

Design rule check (DRC) and Layout vs. Schematic (LVS) tests were performed for verification of the layout. After all optimizations and corrections, the proposed TDC was passed from all these tests, and later on, parasitic extraction simulations were performed. When all of the simulations were repeated with parasitics effects, the propagation delay of the ring oscillator increased up to 31.23 ps. In other words, the effective resolution of the system is decreased. On the other hand, the system keeps its functionality, stability, and linearity without any problem.

The only difference that can be observed during periodic tests is the variation from the

average phase error between successive measurements. Without PEX, variation from the average is ±1 for signals that have 49-50 ns periods. After parasitic extraction, this variation becomes ±2 because of increasing propagation delay. Also, parasitic capacitances change the setup time of the D flip-flops and this phenomenon directly affects the acquisition of phases of the ring oscillator.

Figure 4.21 shows the floorplan of the TDC Top module design. The "Digital Parts" label is used for the combination of all other blocks that are synthesized automatically with the Cadence Encounter tool.

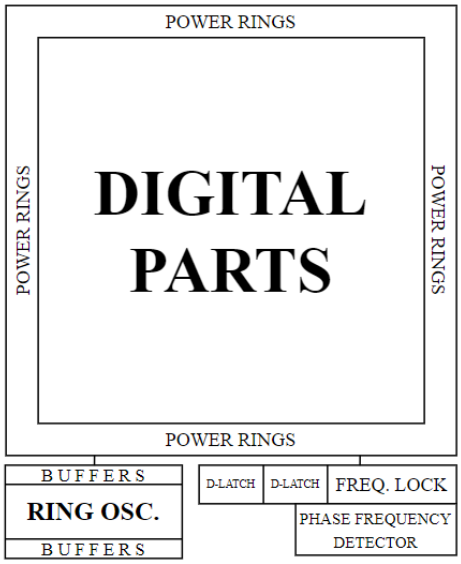

Figure 4.21: Structure of the top module's layout.

4.5. Number of Gates and Area Reports

Table 4.7 shows the area of the layouts of different modules which are synthesized via the Cadence Encounter tool. All dimensions were measured from their place & route boundaries, in other words, results include also the area consumed by power rings. When the overall area of the top module is compared with the area of the core cells, %89.4 density was obtained which is an acceptable ratio. As a result, the proposed TDC was constructed in a 0.057 mm^2 area.

Table 4.7: Layout sizes of the modules.

Name of the Module	Length (µm)	Width (µm)	Area (µm^2)
Multi-input Inverter	5.12	4.19	21.43
31 Phases Ring Oscillator (Core)	15.75	99.78	1571
31 Phases Ring Oscillator (with Buffer Ring)	25.96	109.66	2846.7
Frequency Lock	5	36.72	183.6
Phase-Frequency Detector	16.1	67.1	1080
Digital Parts	191	243.48	46504.6
TDC Top Module	234.13	243.48	57000.2

The number of cells that are utilized for the design is also presented in **Table 4.8**. Area consumptions and number of occurrences of standard cells inside a module can be achieved via gate-area reports which is an analysis of the Cadence synthesis tool. Obtaining this data is significant for calculating and optimizing the density of the overall top module. In total 1850 digital gates were employed to design the overall topology.

Table 4.8: Number of gates used in modules.

Name of the Module	Number of Occurrences in Top Module	Number of the Cells	Area of the Cells
Hamming Distance Block	2	306	11224
Manual Transformation Block	1	221	4100
D-Flip Flop Array (31 Bit)	4	31	8928
D-Flip Flop Array (8 Bit)	4	8	2304
Additional Adders (Automatically Generated)	4	180-200	11210
Error Controller	2	4	236
Frequency Lock	1	4	170
8 Bit Counter	1	72	1625
Phase-Frequency Detector	1	17	716

4.6. Current consumption of the Ring Oscillator and the overall TDC

To determine the adequate widths for power lines, the current consumption of the modules should be investigated. As it was mentioned in the theoretical and experimental part, the biggest contributor to the current consumption is the ring oscillator. Employing

a switch for gating purposes in the design of RO prevents the current flow before resetting. After the system starts the evaluation of the error, the ring oscillator initiates the oscillation and consumes a big portion of the power. However, **Figure 4.22** shows the current consumption of the RO during error measurement in a typical corner.

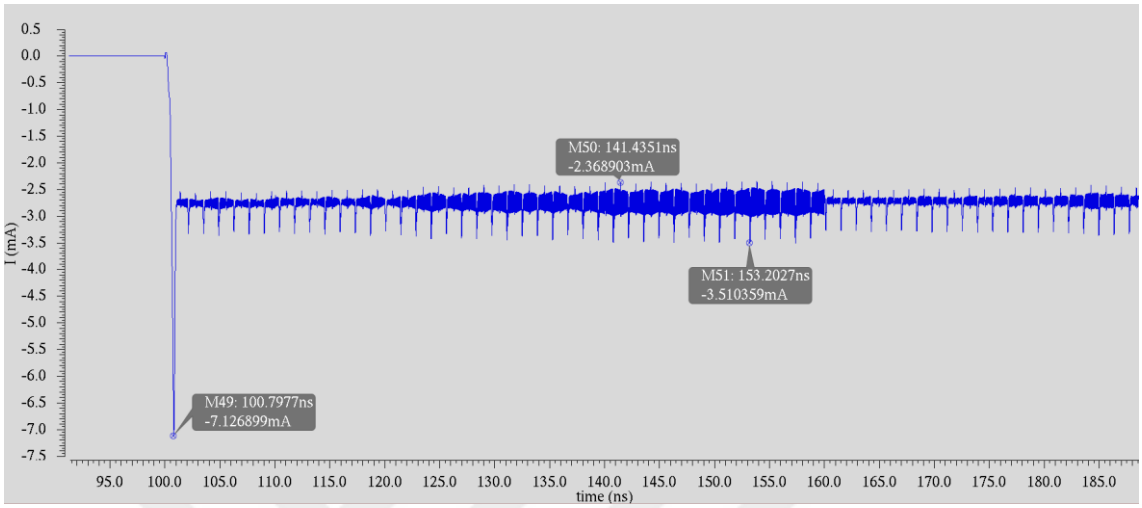

Figure 4.22: Current consumption of the Ring Oscillator.

When the oscillation starts, the inrush current that the oscillator needs to maintain its operation is 7.1 mA. The average current of the ring oscillator is 2.8 mA, with a maximum of 3.5 mA and a minimum of 2.3 mA. Fluctuation in the current causes supply fluctuations as well, which in return affects the oscillation frequency. However, these small disturbances are not significant for the operation of TDC.

Figure 4.23 shows the current consumption of the overall TDC during the same 50 ns time difference.

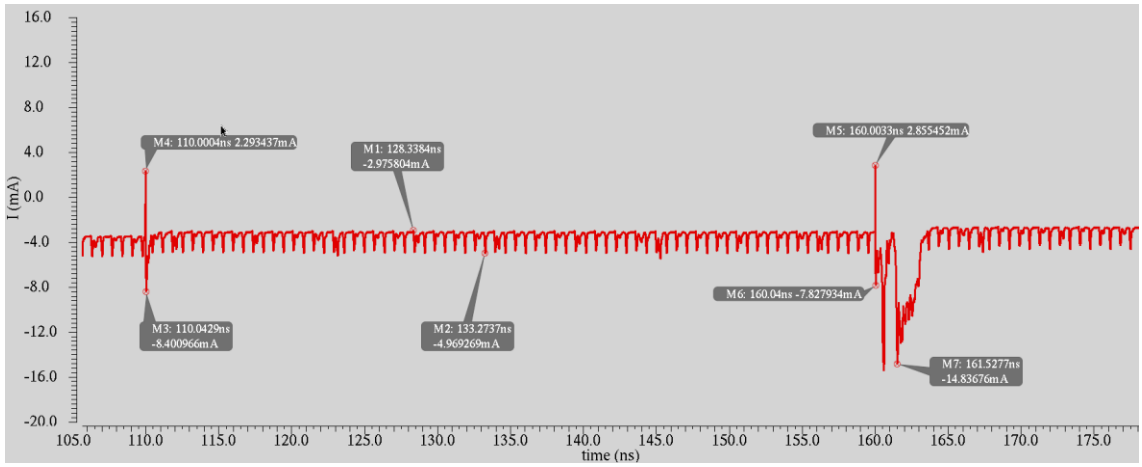

Figure 4.23: Current consumption of the overall TDC.

When the enable and reset signal comes at 100 n, the ring oscillator and all the digital blocks in the TDC start to work, and a small jump occurs as a result of the inrush current. After that, the system stabilizes itself around 3.8 mA and only incoming signals distort the stability of the current consumption. For example, when the reference clock is applied at 110 ns, and the feedback signal at 160 ns, spikes occur in the current graph, but in 10 ps, they return the average. Besides, positive currents are not realistic because the proposed TDC only consumes power, which corresponds to a negative current. To prevent the voltage fluctuations and generation of spurs as a result of current jumps, a low dropout voltage regulator (LDO) was used to supply the TDC.

4.7. Quantization noise calculation of the overall TDC

The quantization noise results that are calculated for different resolutions and reference frequencies are represented in **Table 4.9**. Calculations were done by using equation **3.3** that is presented in the "Experimental Part".

Table 4.9: Quantization noise of the proposed TDC.

CORNERS	PLL_OUT FREQ (MHz)	REF. FREQ (MHz)	NOISE (dBc/Hz)
Typical 22.18 ps	560	20	-105.9
	400	20	-108.8
	560	10	-102.9
	400	10	-105.8
Fastest 12.76 ps	560	20	-110.7
	400	20	-113.6
	560	10	-107.7
	400	10	-110.7
Slowest 31.53 ps	560	20	-102.9
	400	20	-105.8
	560	10	-99.8
	400	10	-102.8

In the worst condition which is the worst speed case in the slow-slow corner, quantization noise increases up to -100 dBc/Hertz. On the other hand, in the best case, the minimum quantization noise that can be achieved is -113.6 dBc/Hertz. Both cases are adequate for the proposed performance parameters of the ADPLL, and loop filters were designed by utilizing these values.

CHAPTER 5

5. CONCLUSIONS AND FUTURE WORK

Phase-locked loops are systems that are used for creating specific frequencies which are multiples of a reference clock frequency. Communication circuits, biomedical, computer sciences, and RF applications are well-known fields that employ PLLs for different purposes. There are 4 main types of PLL that are used to lock specific input signals and they can be listed as Analog PLLs, Digital PLLs, All-Digital PLLs, and Software PLLs. They have many advantages and disadvantages among each other in terms of linearity, resolution, speed, area, and power consumption. However, their working principle is almost the same and highly depends on the utilization of a phase error signal to create a new frequency with voltage-controlled oscillators.

All-digital PLLs employ digitally controlled oscillators to create a signal with a frequency that controlled by digital bits. To measure the phase error between incoming signals and produce these digital control bits, the time difference between reference and feedback phases needs to be digitized. There are many TDC architectures for different applications and the most known types are counter-based TDCs, Flash TDCs, Vernier delay line-based TDCs, and ring oscillator-based TDCs. The most significant parameters that directly indicate the quality of the TDC are linearity, resolution, and dynamic range of the topology. Moreover, area and power consumption are other significant parameters that need to be designed for.

In this thesis, a hybrid time to digital converter was designed in 180nm XFAB CMOS technology. To achieve higher resolutions with low power in a small area, phases of a ring oscillator are employed to create fine distance. The propagation delay between the inverters of the ring oscillator is the main limitation for the resolution, and to increase it, thin-oxide devices were utilized in those inverters. Moreover, instead of using a conventional single input-single output topology, multi-input architecture is employed

which allows the usage of asymmetrical connection of the outputs of inverters to balance the delay times of NMOS and PMOS transistors. Furthermore, a large MOS switch was placed between the main power line and the supply of the ring oscillator for powering down the RO in reset conditions.

The function of the proposed TDC was mimicked on Verilog first to facilitate the error correction process. And once all the tests were completed, codes were transformed to schematic using standard cell library. Phases of the ring oscillator are registered by D-flip flops to compare them with a known reference in hamming distance block which calculates the fine distances for each input signal. After counting periods of the ring oscillator's 0^{th} phase, values were kept by flipflop arrays to form a coarse distance for corresponding input signals. Transformation blocks were designed to combine the fine and the coarse distances to form a 14-bit output which will eventually control the output of the DCO in the PLL loop.

The proposed TDC was verified by functional and periodic tests. These are techniques that show the response of the system for different time intervals in single or repetitive measurements. The resolution of the proposed TDC was obtained as 22.18 ps in a typical corner with 1.8 V supply at room temperature. However, the output of the system was not only investigated in ideal conditions but also examined with ±10% supply voltage variations and different temperatures in the range of -200 to 85 ^{o}C degrees. Due to the voltage, process, and temperature dependence of the propagation delay of the ring oscillator, outputs were obtained differently for each condition, but all results are checked in terms of consistency and no erroneous outcome was obtained. After all the tests were completed successfully, the place and route were performed to obtain the layout for each module. All parts that only contain gates in the standard cell library were synthesized by previously prepared tool command scripts to facilitate the optimization and routing. The proposed TDC was constructed in a 0.057 mm^2 area with %89.4 density. After DRC and LVS checks with Mentor Calibre, parasitics were extracted for post-layout verification. After PEX, the effective propagation delay was increased up to 31.3 ps which is still adequate for the proposed performance parameter. Finally, the proposed TDC was utilized inside a fully functional phase-locked loop to ensure the results and functionality. In the future, the resolution of the system can be increased to decrease quantization noise even further. Moreover, the dead time of the converter can be completely removed by employing parallel conversion units.

BIBLIOGRAPHY

[1] G. C. Hsieh and J. C. Hung, "Phase-locked loop techniques. A survey," *IEEE Trans. Ind. Electron.*, vol. 43, no. 6, pp. 609–615, Dec. 1996, doi: 10.1109/41.544547.

[2] S. C. Gupta, "Phase-Locked Loops," *Proc. IEEE*, vol. 63, no. 2, pp. 291–306, 1975, doi: 10.1109/PROC.1975.9735.

[3] G. A. Leonov, N. V. Kuznetsov, M. V. Yuldashev, and R. V. Yuldashev, "Hold-In, Pull-In, and Lock-In Ranges of PLL Circuits: Rigorous Mathematical Definitions and Limitations of Classical Theory," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 62, no. 10, pp. 2454–2464, Oct. 2015, doi: 10.1109/TCSI.2015.2476295.

[4] J. H. Vincent, "On some Experiments in which Two Neighbouring maintained Oscillatory Circuits affect a Resonating Circuit," *Proc. Phys. Soc. London*, vol. 32, no. 1, pp. 84–91, Dec. 1919, doi: 10.1088/1478-7814/32/1/311.

[5] J. Henderson, 059 CM Wine - US Patent 4, 106, and U. 1978, "Phase locked loop television tuning system," 1978.

[6] A. Grebene and H. Camenzind, "Phase locking as a new approach for tuned integrated circuits," in *1969 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, 1969, pp. 100–101, doi: 10.1109/ISSCC.1969.1154749.

[7] B. B. Purkayastha and K. K. Sarma, *A Digital Phase Locked Loop based Signal and Symbol Recovery System for Wireless Channel*, no. October. 2015.

[8] R. Tonietto, E. Zuffetti, R. Castello, and I. Bietti, "A 3MHz Bandwidth Low Noise RF All Digital PLL with 12ps Resolution Time to Digital Converter," in *2006 Proceedings of the 32nd European Solid-State Circuits Conference*, Sep. 2006, pp. 150–153, doi: 10.1109/ESSCIR.2006.307553.

[9] X. Wang and T. Kwasniewski, "A Static Phase Offset Reduction Technique for Multiplying Delay-Locked Loop," *Circuits Syst.*, vol. 06, no. 01, pp. 13–19, 2015, doi: 10.4236/cs.2015.61002.

[10] P. Heydari, "Analysis of the PLL Jitter Due to Power/Ground and Substrate Noise," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 51, no. 12, pp. 2404–2416, Dec. 2004, doi: 10.1109/TCSI.2004.838240.

[11] Heng-Chia Chang, "Phase noise in self-injection-locked oscillators - Theory and experiment," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 9, pp. 1994–1999, Sep. 2003, doi: 10.1109/TMTT.2003.815872.

[12] G. Pasternack and R. L. Whalin, "Analysis and Synthesis of a Digital Phase-Locked Loop for FM Demodulation," *Bell Syst. Tech. J.*, vol. 47, no. 10, pp. 2207–2237, 1968, doi: 10.1002/j.1538-7305.1968.tb01083.x.

[13] W. Lindsey and M. . Simon, *Phase-locked loops and their application*. New York, 1978.

[14] M. Karimi-Ghartemani, H. Karimi, and M. R. Iravani, "A Magnitude/Phase-Locked Loop System Based on Estimation of Frequency and In-

Phase/Quadrature-Phase Amplitudes," *IEEE Trans. Ind. Electron.*, vol. 51, no. 2, pp. 511–517, Apr. 2004, doi: 10.1109/TIE.2004.825282.

[15] R. Dixon, "Radio Receiver Design," Nature, vol. 157, no. 3997, pp. 751–751, Jun. 1946, doi: 10.1038/157751b0.

[16] D. Jeong, G. Borriello, D. A. Hodges, and R. H. Katz, "Design of PLL-based clock generation circuits," *IEEE J. Solid-State Circuits*, vol. 22, no. 2, pp. 255–261, Apr. 1987, doi: 10.1109/JSSC.1987.1052710.

[17] M. Hsieh and G. Sobelman, "Architectures for multi-gigabit wire-linked clock and data recovery," *IEEE Circuits Syst. Mag.*, vol. 8, no. 4, pp. 45–57, 2008, doi: 10.1109/MCAS.2008.930152.

[18] M. Horowitz, Chih-Kong Ken Yang, and S. Sidiropoulos, "High-speed electrical signaling: overview and limitations," *IEEE Micro*, vol. 18, no. 1, pp. 12–24, 1998, doi: 10.1109/40.653013.

[19] W. Rodda, E. Campbell, D. J. Sauer, W. T. Mayweather, and F. Dell'ova, "Full CMOS video line-locked phase-locked loop system," *IEEE Trans. Consum. Electron.*, vol. 39, no. 3, pp. 496–503, 1993, doi: 10.1109/30.234626.

[20] T. Olsson and P. Nilsson, "An all-digital PLL clock multiplier," in *Proceedings. IEEE Asia-Pacific Conference on ASIC*, 2002, pp. 275–278, doi: 10.1109/APASIC.2002.1031585.

[21] Á. M. Bueno, J. M. Balthazar, and J. R. C. Piqueira, "Phase-Locked Loop design applied to frequency-modulated atomic force microscope," *Commun. Nonlinear Sci. Numer. Simul.*, vol. 16, no. 9, pp. 3835–3843, Sep. 2011, doi: 10.1016/j.cnsns.2010.12.018.

[22] T. Li, J. Zhou, S. Liu, J. Shi, and F. Ren, "Phase- Locked Loop Based Cancellation of ECG Power Line Interference," *Ztecommunications*, vol. 16, pp. 47–51, 2020, doi: 10.3969/J.ISSN.1673-5188.2018.01.008.

[23] G. Bischof, B. Scholnick, and E. Salman, "Fully integrated PLL based clock generator for implantable biomedical applications," in *2011 IEEE Long Island Systems, Applications and Technology Conference*, May 2011, pp. 1–6, doi: 10.1109/LISAT.2011.5784225.

[24] V. Prasad and C. Sharma, "A Review of Phase Locked Loop," *Int. J. Emerg. Technol. Adv. Eng.*, vol. 2, no. 6, pp. 98–104, 2012.

[25] C.-M. Hsu, M. Z. Straayer, and M. H. Perrott, "A Low-Noise Wide-BW 3.6-GHz Digital Delta\Sigma Fractional-N Frequency Synthesizer With a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2776–2786, Dec. 2008, doi: 10.1109/JSSC.2008.2005704.

[26] Analaog Devices, "MT-086 Tutorial - Fundamentals of Phase Locked Loops (PLLs)," 1st ed., 2017.

[27] S. Soliman, F. Yuan, and K. Raahemifar, "An overview of design techniques for CMOS phase detectors," in *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*, 2002, vol. 5, pp. V-457-V–460, doi: 10.1109/ISCAS.2002.1010739.

[28] B. Chakraborty and R. R. Pal, “Design of a Phase Detector with Improved Performance,” *Physics (College. Park. Md).*, vol. 12, pp. 213–220, 2008.

[29] O. Kazanc, “High Frequency Low-Jitter Phase-Locked Loop Design,”Yeditepe University, Istanbul, Engineering Project Report, 2008.

[30] K. Shu, E. Sanchez-Sinencio, J. Silva-Martinez, and S. H. K. Embabi, “A 2.4-GHz monolithic fractional-N frequency synthesizer with robust phase-switching prescaler and loop capacitance multiplier,” *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 866–874, Jun. 2003, doi: 10.1109/JSSC.2003.811875.

[31] Y. Chou, Y. Chen, W. L. Mao, and F. R. Chang, “Loop filter design for phase-locked loops with delay: A multi-objective control approach,” in *2007 European Control Conference (ECC)*, Jul. 2007, pp. 984–991, doi: 10.23919/ECC.2007.7068703.

[32] P. Andreani and S. Mattisson, “On the use of MOS varactors in RF VCOs,” *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 905–910, Jun. 2000, doi: 10.1109/4.845194.

[33] B. Kinger, S. Suman, K. G. Sharma, and P. K. Ghosh, “Design of Improved Performance Voltage Controlled Ring Oscillator,” in *2015 Fifth International Conference on Advanced Computing & Communication Technologies*, Feb. 2015, pp. 441–445, doi: 10.1109/ACCT.2015.127.

[34] Zhenbiao Li and K. K. O, “A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator,” *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1296–1302, Jun. 2005, doi: 10.1109/JSSC.2005.848031.

[35] U. Singh and M. M. Green, “High-frequency CML clock dividers in 0.13 um CMOS operating up to 38 GHz,” *IEEE J. Solid-State Circuits*, vol. 40, no. 8, pp. 1658–1661, Aug. 2005, doi: 10.1109/JSSC.2005.852420.

[36] B. Blalock and E. Farquhar, “Design and Analysis of a Delta Sigma Modulator for a Fractional N Phase Locked Loop Frequency Synthesizer Operating at 2 . 4 GHz A Thesis Presented for the Master of Science Degree The University of Tennessee , Knoxville Timothy Richard Grundman May 2008,” 2008.

[37] A. Godave, P. Choudhari, and A. Jadhav, “Comparison and Simulation of Analog and Digital Phase Locked Loop,” in *2018 9th International Conference on Computing, Communication and Networking Technologies (ICCCNT)*, Jul. 2018, pp. 1–4, doi: 10.1109/ICCCNT.2018.8494198.

[38] R. B. Staszewski and P. T. Balsara, “All-digital PLL with ultra fast settling,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 54, no. 2, pp. 181–185, Feb. 2007, doi: 10.1109/TCSII.2006.886896.

[39] R. E. Best, “Introduction to PLLs” in *Phase-locked loops: design, simulation, and applications*. 6th ed., McGraw-Hill Education., 2007, pp. 1-8.

[40] A. Singhal, C. Madhu, and V. Kumar, “Designs of All Digital Phase Locked Loop,” in *2014 Recent Advances in Engineering and Computational Sciences (RAECS)*, Mar. 2014, pp. 1–5, doi: 10.1109/RAECS.2014.6799523.

[41] B. Razavi, *Design of Analog CMOS Integrated Circuits* - Tata McGraw-Hill Education, 2002 ISSN: 978-0-07-252493-2.

[42] C. Jiang, P. Andreani, and U. D. Keil, “Detailed Behavioral Modeling of Bang-Bang Phase Detectors,” in *APCCAS 2006 - 2006 IEEE Asia Pacific Conference on Circuits and Systems*, Dec. 2006, pp. 716–719, doi: 10.1109/APCCAS.2006.342108.

[43] X. Chen, J. Yang, and X. Deng, “A Contribution to the Discrete Z-Domain Analysis of ADPLL,” in *2007 7th International Conference on ASIC*, Oct. 2007, pp. 185–188, doi: 10.1109/ICASIC.2007.4415598.

[44] X. Chen, J. Yang, and L.-X. Shi, “A Fast Locking All-Digital Phase-Locked Loop via Feed-Forward Compensation Technique,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 19, no. 5, pp. 857–868, May 2011, doi: 10.1109/TVLSI.2009.2039971.

[45] Z. Cheng, X. Zheng, M. J. Deen, and H. Peng, “Recent Developments and Design Challenges of High-Performance Ring Oscillator CMOS Time-to-Digital Converters,” *IEEE Trans. Electron Devices*, vol. 63, no. 1, pp. 235–251, Jan. 2016, doi: 10.1109/TED.2015.2503718.

[46] G. Clark, *Bruno Benedetto Rossi, 13 April 1905· 21 November 1993*. 2000.

[47] Y.Arai, T.Baba, “A CMOS time to digital converter VLSI for high-energy physics,” in *Symposium on VLSI Circuits*, 1988, pp. 121–122, doi: 10.1109/VLSIC.1988.1037453.

[48] V. Nguyen, D. Duong, Y. Chung, and J.-W. Lee, “A Cyclic Vernier Two-Step TDC for High Input Range Time-of-Flight Sensor Using Startup Time Correction Technique,” *Sensors*, vol. 18, no. 11, p. 3948, Nov. 2018, doi: 10.3390/s18113948.

[49] W. Rhee, *Phase-Locked Frequency Generation and Clocking: Architectures and circuits for modern wireless and wireline systems (Materials, Circuits and Devices)*. 2020.

[50] E. Venialgo *et al.*, “Toward a Full-Flexible and Fast-Prototyping TOF-PET Block Detector Based on TDC-on-FPGA,” *IEEE Trans. Radiat. Plasma Med. Sci.*, vol. 3, no. 5, pp. 538–548, Sep. 2019, doi: 10.1109/TRPMS.2018.2874358.

[51] S. Henzler, S. Koeppe, D. Lorenz, W. Kamp, R. Kuenemund, and D. Schmitt-Landsiedel, “A Local Passive Time Interpolation Concept for Variation-Tolerant High-Resolution Time-to-Digital Conversion,” *IEEE J. Solid-State Circuits*, vol. 43, no. 7, pp. 1666–1676, Jul. 2008, doi: 10.1109/JSSC.2008.922712.

[52] P. Madoglio, M. Zanuso, S. Levantino, C. Samori, and A. L. Lacaita, “Quantization Effects in All-Digital Phase-Locked Loops,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 54, no. 12, pp. 1120–1124, Dec. 2007, doi: 10.1109/TCSII.2007.906171.

[53] D. Osipov, H. Lange, and S. Paul, “International Journal of Electronics Energy-efficient CMOS delay line with self-supply modulation for low-power SAR ADCs Energy-efficient CMOS delay line with self-supply modulation for low-power SAR ADCs,” *Taylor Fr.*, vol. 107, no. 3, pp. 403–416, Mar. 2019, doi: 10.1080/00207217.2019.1661024.

[54] N. Narku-Tetteh, A. Titriku, and S. Palermo, “A 15b, Sub-10ps resolution, low dead time, wide range two-stage TDC,” in *2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Aug. 2014, pp. 13–16, doi: 10.1109/MWSCAS.2014.6908340.

[55] A. S. Yousif and J. W. Haslett, “A Fine Resolution TDC Architecture for Next Generation PET Imaging,” *IEEE Trans. Nucl. Sci.*, vol. 54, no. 5, pp. 1574–1582, Oct. 2007, doi: 10.1109/TNS.2007.903183.

[56] L. H. C. Braga *et al.*, “A fully digital 8×16 sipm array for pet applications with per-pixel tdcs and real-time energy output,” *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 301–314, Jan. 2014, doi: 10.1109/JSSC.2013.2284351.

[57] N. G. Abdallah, M. Rashdan, and A. A. M. Khalaf, “High Resolution Time-to-digital Converter for PET Imaging,” in *2020 International Conference on Innovative Trends in Communication and Computer Engineering (ITCE)*, Feb. 2020, pp. 295–298, doi: 10.1109/ITCE48509.2020.9047816.

[58] S. Tancock, E. Arabul, and N. Dahnoun, “A Review of New Time-to-Digital Conversion Techniques,” *IEEE Trans. Instrum. Meas.*, vol. 68, no. 10, pp. 3406–3417, Oct. 2019, doi: 10.1109/TIM.2019.2936717.

[59] M. A. Ozdemir and A. Tangel, “VLSI Implementation of TDC Architectures Used in PET Imaging Systems,” Jun. 2020, arxiv:2006.06034.

[60] C. S. Hoaglund, S. J. Valentine, C. R. Sporleder, J. P. Reilly, and D. E. Clemmer, “Three-Dimensional Ion Mobility/TOFMS Analysis of Electrosprayed Biomolecules,” *Anal. Chem.*, vol. 70, no. 11, pp. 2236–2242, Jun. 1998, doi: 10.1021/ac980059c.

[61] L. Wei and D. Ho, “Recent Advances in Fluorescence Lifetime Analytical Microsystems: Contact Optics and CMOS Time-Resolved Electronics,” *Sensors*, vol. 17, no. 12, p. 2800, Dec. 2017, doi: 10.3390/s17122800.

[62] S. Lindner, C. Zhang, I. M. Antolovic, M. Wolf, and E. Charbon, “A 252 × 144 SPAD Pixel Flash Lidar with 1728 Dual-Clock 48.8 PS TDCs, Integrated Histogramming and 14.9-to-1 Compression in 180NM CMOS Technology,” in *2018 IEEE Symposium on VLSI Circuits*, Jun. 2018, pp. 69–70, doi: 10.1109/VLSIC.2018.8502386.

[63] S. Lee, D. Lee, P. Choi, and D. Park, “Accuracy–Power Controllable LiDAR Sensor System with 3D Object Recognition for Autonomous Vehicle,” *Sensors*, vol. 20, no. 19, p. 5706, Oct. 2020, doi: 10.3390/s20195706.

[64] B. Markovic, S. Tisa, F. A. Villa, A. Tosi, and F. Zappa, “A High-Linearity, 17 ps Precision Time-to-Digital Converter Based on a Single-Stage Vernier Delay Loop Fine Interpolation,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 60, no. 3, pp. 557–569, Mar. 2013, doi: 10.1109/TCSI.2012.2215737.

[65] F. Yuan, “CMOS time-to-digital converters for mixed-mode signal processing,” *J. Eng.*, vol. 2014, no. 4, pp. 140–154, Apr. 2014, doi: 10.1049/joe.2014.0044.

[66] B. Ghanavati, E. Abiri, N. Azhdari, and M. R. Salehi, “A TLBO Optimized TDC for Biomedical Applications,” in *Electrical Engineering (ICEE), Iranian Conference on*, May 2018, pp. 76–80, doi: 10.1109/ICEE.2018.8472459.

[67] M. Jurgo “Structure of All-Digital Frequency Synthesiser for IoT and IoV Applications,” *Electronics*, vol. 8, no. 1, p. 29, Dec. 2018.

[68] Z. Soni, A. Patel, D. K. Panda, and A. B. Sarbadhikari, “Comparative Study of Delay Line Based Time to Digital Converter Using FPGA,” *Int. Res. J. Eng. Technol.*, vol. 4, no. 9, pp. 1169–1175, 2017.

[69] Z. Xu, M. Miyahara, K. Okada, and A. Matsuzawa, “A 3.6 GHz Low-Noise Fractional-N Digital PLL Using SAR-ADC-Based TDC,” *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2345–2356, Oct. 2016, doi: 10.1109/JSSC.2016.2582854.

[70] E. Raisanen-Ruotsalainen, T. Rahkonen, and J. Kostamovaara, “A high resolution time-to-digital converter based on time-to-voltage interpolation,” *Proc. 23rd Eur. Solid-State Circuits Conf.*, pp. 2–5, 1997, doi: 10.1109/ESSCIR.1997.186174.

[71] C.-C. Lin, C.-H. Weng, T.-A. Wei, Y.-Y. Lin, and T.-H. Lin, “A TDC-Based Two-Step Quantizer With Swapper Technique for a Multibit Continuous-Time Delta–Sigma Modulator,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 61, no. 2, pp. 75–79, Feb. 2014, doi: 10.1109/TCSII.2013.2291138.

[72] D. Sheng, C. Chung, C. Huang, and J. Jian, “A high-resolution and one-cycle conversion time-to-digital converter architecture for PET image applications,” in *2013 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, Jul. 2013, pp. 2461–2464, doi: 10.1109/EMBC.2013.6610038.

[73] S. Henzler, “*Time-to-Digital Converter Basics,*” Springer, 2010, pp. 5–18.

[74] B. I. Abdulrazzaq, I. Abdul Halin, S. Kawahito, R. M. Sidek, S. Shafie, and N. A. M. Yunus, “A review on high-resolution CMOS delay lines: towards sub-picosecond jitter performance,” *SpringerPlus*, vol. 5, no. 1. SpringerOpen, Dec. 01, 2016, doi: 10.1186/s40064-016-2090-z.

[75] M. Z. Straayer and M. H. Perrott, “A Multi-Path Gated Ring Oscillator TDC With First-Order Noise Shaping,” *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, Apr. 2009, doi: 10.1109/JSSC.2009.2014709.

[76] R. Narasimman, A. Prabhakar, and N. Chandrachoodan, “Implementation of a 30 ps resolution time to digital converter in FPGA,” in *2015 International Conference on Electronic Design, Computer Networks & Automated Verification (EDCAV)*, Jan. 2015, pp. 12–17, doi: 10.1109/EDCAV.2015.7060530.

[77] H. Wang, M. Zhang, and Y. Liu, “High-Resolution Digital-to-Time Converter Implemented in an FPGA Chip,” *Appl. Sci.*, vol. 7, no. 1, p. 52, Jan. 2017, doi: 10.3390/app7010052.

[78] G. H. Li and H. P. Chou, “A high resolution time-to-digital converter using two-level vernier delay line technique,” in *2007 IEEE Nuclear Science Symposium Conference Record*, Oct. 2007, pp. 276–280, doi: 10.1109/NSSMIC.2007.4436330.

[79] M. Alioto and G. Palumbo, “Oscillation frequency in CML and ESCL ring oscillators,” *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 48, no. 2,

pp. 210–214, 2001, doi: 10.1109/81.904885.

[80] A. J. Mondal, J. Talukdar, and B. K. Bhattacharyya, “Estimation of frequency and amplitude of ring oscillator built using current sources,” *Ain Shams Eng. J.*, vol. 11, no. 3, pp. 677–686, Sep. 2020, doi: 10.1016/j.asej.2020.01.006.

[81] K.-C. Choi, S.-W. Lee, B.-C. Lee, and W.-Y. Choi, “A Time-to-Digital Converter Based on a Multiphase Reference Clock and a Binary Counter With a Novel Sampling Error Corrector,” *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 59, no. 3, pp. 143–147, Mar. 2012, doi: 10.1109/TCSII.2012.2184370.

[82] J. Yu, F. F. Dai, and R. C. Jaeger, “A 12-Bit Vernier Ring Time-to-Digital Converter in 0.13 um CMOS Technology,” *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 830–842, Apr. 2010, doi: 10.1109/JSSC.2010.2040306.

[83] M. K. Mandal and C. Sarkar, “Ring oscillators: Characteristics and applications,” *Indian J. Pure Appl. Phys.*, vol. 48, pp. 136–145, 2010.

[84] S. J. Lee, B. Kim, and K. Lee, “A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme,” *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 289–291, 1997, doi: 10.1109/4.551926.

[85] M. M. Sorkhabi and S. Toofan, “A high resolution, multi-path gated ring oscillator based Vernier Time-to-Digital Converter,” in *2011 Semiconductor Conference Dresden*, Sep. 2011, pp. 1–4, doi: 10.1109/SCD.2011.6068695.

[86] P. Lu, A. Liscidini, and P. Andreani, “A 3.6 mW, 90 nm CMOS Gated-Vernier Time-to-Digital Converter With an Equivalent Resolution of 3.2 ps,” *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1626–1635, Jul. 2012, doi: 10.1109/JSSC.2012.2191676.

[87] W.-H. Lee, B.-J. Gu, Y. Nishida, H. Takao, K. Sawada, and M. Ishida, “Oscillation-controlled CMOS ring oscillator for wireless sensor systems,” *Microelectronics J.*, vol. 41, no. 12, pp. 815–819, Dec. 2010, doi: 10.1016/j.mejo.2010.07.002.

[88] Z. Cheng, M. J. Deen, and H. Peng, “A Low-Power Gateable Vernier Ring Oscillator Time-to-Digital Converter for Biomedical Imaging Applications,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 2, pp. 445–454, Apr. 2016, doi: 10.1109/TBCAS.2015.2434957.

[89] H. Wang, F. F. Dai, and H. Wang, “A 330μW 1.25ps 400fs-INL vernier time-to-digital converter with 2D reconfigurable spiral arbiter array and 2 nd -order ΔΣ linearization,” in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, Apr. 2017, pp. 1–4, doi: 10.1109/CICC.2017.7993635.

[90] P. Lu, A. Liscidini, and P. Andreani, “A 2-D GRO Vernier time-to-digital converter with large input range and small latency,” *Analog Integr. Circuits Signal Process.*, vol. 76, no. 2, pp. 195–206, Aug. 2013, doi: 10.1007/s10470-13-0084-0.

[91] L. Vercesi, A. Liscidini, and R. Castello, “Two-Dimensions Vernier Time-to-Digital Converter,” *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1504–1512, Aug. 2010, doi: 10.1109/JSSC.2010.2047435.

[92] P. Lu and P. Andreani, “A 1-1 MASH 2-D vernier time-to-digital converter with 2nd-order noise shaping,” in *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, Jun. 2014, pp. 1324–1327, doi: 10.1109/ISCAS.2014.6865387.

[93] H. Wang and F. F. Dai, “A 14-Bit, 1-ps resolution, two-step ring and 2D Vernier TDC in 130nm CMOS technology,” in *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, Sep. 2017, pp. 143–146, doi: 10.1109/ESSCIRC.2017.8094546.

[94] B. Kim, H. Kim, and C. H. Kim, “An 8bit, 2.6ps two-step TDC in 65nm CMOS employing a switched ring-oscillator based time amplifier,” in *2015 IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2015, pp. 1–4, doi: 10.1109/CICC.2015.7338425.

[95] T. Oh, H. Venkatram, and U.-K. Moon, “A Time-Based Pipelined ADC Using Both Voltage and Time Domain Information,” *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 961–971, Apr. 2014, doi: 10.1109/JSSC.2013.2293019.

[96] K.-C. Chao, J.-C. Lai, and T.-Y. Hsu, “All-Digital Mismatched Calibrator and Compensator for SR Latch-Based Variable-Gain Time Amplifier,” *IEEE Access*, vol. 8, pp. 42082–42096, 2020, doi: 10.1109/ACCESS.2020.2977861.

[97] K. Kim, Y.-H. Kim, W. Yu, and S. Cho, “A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier,” *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1009–1017, Apr. 2013, doi: 10.1109/JSSC.2013.2237996.

[98] M. Lee and A. A. Abidi, “A 9b, 1.25ps Resolutilon Coarse-Fine Time-to-Digital Converter in 90nm CMOS that Amplifies a Time Residue,” in *2007 IEEE Symposium on VLSI Circuits*, Jun. 2007, pp. 168–169, doi: 10.1109/VLSIC.2007.4342701.

[99] R. Enomoto, T. Iizuka, T. Koga, T. Nakura, and K. Asada, “A 16-bit 2.0-ps Resolution Two-Step TDC in 0.18-um CMOS Utilizing Pulse-Shrinking Fine Stage With Built-In Coarse Gain Calibration,” *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 27, no. 1, pp. 11–19, Jan. 2019, doi: 10.1109/TVLSI.2018.2867505.

[100] M. Rashdan, “Multi-step and high-resolution vernier-based TDC architecture,” in *2017 29th International Conference on Microelectronics (ICM)*, Dec. 2017, pp. 1–4, doi: 10.1109/ICM.2017.8268819.

[101] R. Razmdideh, M. S.-I. J. of Circuit, and undefined 2018, “Low-power, latch-based multistage time-to-digital converter in 65 nm CMOS technology,” *Wiley Online Libr.*, vol. 46, no. 6, pp. 1264–1271, Jun. 2018, doi: 10.1002/cta.2468.

[102] M. Fishburn, L. H. Menninga, C. Favi, and E. Charbon, “A 19.6 ps, FPGA-Based TDC With Multiple Channels for Open Source Applications,” *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 2203–2208, Jun. 2013, doi: 10.1109/TNS.2013.2241789.

[103] M. Zieliński, “Review of single-stage time-interval measurement modules implemented in FPGA devices,” *Metrol. Meas. Syst* vol.16, no. 4, pp. 641-647, 2009.

[104] H. Chen and D. D.-U. Li, “Multichannel, Low Nonlinearity Time-to-Digital Converters Based on 20 and 28 nm FPGAs,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 3265–3274, Apr. 2019, doi: 10.1109/TIE.2018.2842787.

[105] J. Y. Won, S. Il Kwon, H. S. Yoon, G. B. Ko, J.-W. Son, and J. S. Lee, “Dual-Phase Tapped-Delay-Line Time-to-Digital Converter With On-the-Fly Calibration Implemented in 40 nm FPGA,” *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 1, pp. 231–242, Feb. 2016, doi: 10.1109/TBCAS.2015.2389227.

[106] J. Y. Won and J. S. Lee, “Time-to-Digital Converter Using a Tuned-Delay Line Evaluated in 28-, 40-, and 45-nm FPGAs,” *IEEE Trans. Instrum. Meas.*, vol. 65, no. 7, pp. 1678–1689, Jul. 2016, doi: 10.1109/TIM.2016.2534670.

[107] C. Hervé, J. Cerrai, and T. Le Caër, “High resolution time-to-digital converter (TDC) implemented in field programmable gate array (FPGA) with compensated process voltage and temperature (PVT) variations,” *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, vol. 682, pp. 16–25, Aug. 2012, doi: 10.1016/j.nima.2012.04.040.

[108] W. Pan, G. Gong, and J. Li, “A 20-ps Time-to-Digital Converter (TDC) Implemented in Field-Programmable Gate Array (FPGA) with Automatic Temperature Correction,” *IEEE Trans. Nucl. Sci.*, vol. 61, no. 3, pp. 1468–1473, Jun. 2014, doi: 10.1109/TNS.2014.2320325.

[109] P. Keranen and J. Kostamovaara, “Algorithmic time-to-digital converter,” in *2013 NORCHIP*, Nov. 2013, pp. 1–4, doi: 10.1109/NORCHIP.2013.6702022.

[110] P. Keranen and J. Kostamovaara, “A Wide Range, 4.2 ps(rms) Precision CMOS TDC With Cyclic Interpolators Based on Switched-Frequency Ring Oscillators,” *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 62, no. 12, pp. 2795–2805, Dec. 2015, doi: 10.1109/TCSI.2015.2485719.

[111] M. H. Perrott, "Tutorial on digital phase-locked loops.", Custom Integrated Circuits Conference CCIC, 2009.

APPENDIX A

Appendix A1. Verilog code of the 31 Phases Ring Oscillator

```
`timescale 1ns / 1fs

module ring_osc_31ph (clk,rstb) ;
 output [30:0] clk ;
 input rstb ;
 wire [30:0] clk ;
 real ctrl_delay;
 real f_dco  = 0.896;

 always @(*)

  ctrl_delay = 1 / (62*f_dco);

  assign #(ctrl_delay) clk[ 1] = ~clk[ 0] | ~rstb ;
  assign #(ctrl_delay) clk[ 2] = ~clk[ 1] ;
  assign #(ctrl_delay) clk[ 3] = ~clk[ 2] ;
  assign #(ctrl_delay) clk[ 4] = ~clk[ 3] ;
  assign #(ctrl_delay) clk[ 5] = ~clk[ 4] ;
  assign #(ctrl_delay) clk[ 6] = ~clk[ 5] ;
  assign #(ctrl_delay) clk[ 7] = ~clk[ 6] ;
  assign #(ctrl_delay) clk[ 8] = ~clk[ 7] ;
  assign #(ctrl_delay) clk[ 9] = ~clk[ 8] ;
  assign #(ctrl_delay) clk[10] = ~clk[ 9] ;
  assign #(ctrl_delay) clk[11] = ~clk[10] ;
  assign #(ctrl_delay) clk[12] = ~clk[11] ;
  assign #(ctrl_delay) clk[13] = ~clk[12] ;
  assign #(ctrl_delay) clk[14] = ~clk[13] ;
  assign #(ctrl_delay) clk[15] = ~clk[14] ;
  assign #(ctrl_delay) clk[16] = ~clk[15] ;
  assign #(ctrl_delay) clk[17] = ~clk[16] ;
  assign #(ctrl_delay) clk[18] = ~clk[17] ;
  assign #(ctrl_delay) clk[19] = ~clk[18] ;
  assign #(ctrl_delay) clk[20] = ~clk[19] ;
  assign #(ctrl_delay) clk[21] = ~clk[20] ;
  assign #(ctrl_delay) clk[22] = ~clk[21] ;
  assign #(ctrl_delay) clk[23] = ~clk[22] ;
  assign #(ctrl_delay) clk[24] = ~clk[23] ;
  assign #(ctrl_delay) clk[25] = ~clk[24] ;
  assign #(ctrl_delay) clk[26] = ~clk[25] ;
  assign #(ctrl_delay) clk[27] = ~clk[26] ;
  assign #(ctrl_delay) clk[28] = ~clk[27] ;
  assign #(ctrl_delay) clk[29] = ~clk[28] ;
  assign #(ctrl_delay) clk[30] = ~clk[29] ;
  assign #(ctrl_delay) clk[ 0] = ~clk[30] ;

endmodule
```

Appendix A2. Verilog code of the Hamming Distance Block

```
module hamming_with_error28(distance,phase,errc1);

output reg signed[6:0] distance;
input [30:0] phase ;
reg [6:0] primary_distance;
input errc1;
reg error1;
always @(*)
begin
primary_distance = (phase[ 0]^1'b1) + (phase[ 1]^1'b1) +
(phase[ 2]^1'b0) + (phase[ 3]^1'b1) + (phase[ 4]^1'b0) +
(phase[ 5]^1'b1) + (phase[ 6]^1'b0) + (phase[ 7]^1'b1) +
(phase[ 8]^1'b0) + (phase[ 9]^1'b1) + (phase[10]^1'b0) +   (phase[11]^1'b1) +
(phase[12]^1'b0) + (phase[13]^1'b1) + (phase[14]^1'b0) + (phase[15]^1'b1) +
(phase[16]^1'b0) + (phase[17]^1'b1) + (phase[18]^1'b0) + (phase[19]^1'b1) +
(phase[20]^1'b0) + (phase[21]^1'b1) + (phase[22]^1'b0) + (phase[23]^1'b1) +
(phase[24]^1'b0) + (phase[25]^1'b1) + (phase[26]^1'b0) + (phase[27]^1'b1) +
(phase[28]^1'b0) + (phase[29]^1'b1) + (phase[30]^1'b0) ;

error1 = ~(errc1 | phase[28]);
  if (phase[0] == 1'b1)
     distance = primary_distance ;
  else if (error1)
     distance = 6'd0  - primary_distance ;
  else
     distance = 6'd62 - primary_distance ;
end
endmodule
```

Appendix A3. Verilog code of the Manual Transformation Block

```
module
manual_transformation_block_v9(hd1,hd2,coarse1,coarse2,manually_signed_fine_dista
nce,new_coarse_distance);

input  [7:0]  coarse1,coarse2;
input  signed[6:0]  hd1,hd2;
wire   signed[7:0]  hd_dif;
wire   [7:0]  coarse_dif;
output signed[13:0] manually_signed_fine_distance;
output signed[13:0] new_coarse_distance;

assign hd_dif  = hd2-hd1;
assign coarse_dif       = coarse2-coarse1;
assign new_coarse_distance = 6'd62 *
{coarse_dif[7],coarse_dif[7],coarse_dif[7],coarse_dif[7],coarse_dif[7],coarse_dif[7],
coarse_dif};
assign manually_signed_fine_distance   =
```

```
{hd_dif[7],hd_dif[7],hd_dif[7],hd_dif[7],hd_dif[7],hd_dif[7],hd_dif};

endmodule
```

Appendix A4. Verilog code of the Phase Frequency Detector

```
`timescale 1ns/1fs
module phase_frequency_detector(t1u,t2d,ck_loop,ck_ref,ck_div,rstb);

output reg t1u,t2d;
output ck_loop;
input ck_ref,ck_div,rstb;
wire rst;
always @(posedge ck_ref or posedge rst)

        if(rst)
                t1u<=1'b0;
        else
                t1u<=1'b1;

always @(posedge ck_div or posedge rst)

        if(rst)
                t2d<=1'b0;
        else
                t2d<=1'b1;

assign #(0.5) rst = ((t1u && t2d) || (~rstb));
assign ck_loop    = ~(t1u & t2d);

endmodule
```

Appendix A5. Verilog code of the Frequency Detector (Lock)

```
`timescale 1ns/1fs
module frequency_lock (freq_lock, t1u, t2d, clk_ref, clk_div, rstb) ;
  output freq_lock ;
  input t1u, t2d ;
  input clk_ref, clk_div, rstb ;

  reg t1u_ctrl, t2d_ctrl ;

  always @(posedge clk_ref or negedge rstb)
    if (rstb == 0)
      t1u_ctrl <= 1'b1 ;
    else
      t1u_ctrl <= t1u ;

  always @(posedge clk_div or negedge rstb)
```

```
   if (rstb == 0)
     t2d_ctrl <= 1'b1 ;
   else
     t2d_ctrl <= t2d ;

  assign freq_lock = ~(t1u_ctrl | t2d_ctrl) ;
endmodule
```

Appendix A6. Verilog code of the Error Controller

```
module error_controller_ref(error_ref,ck_loop_dly,sync_clk_ref,clk_ref,clk_ro,rstb);

output error_ref;
input ck_loop_dly,sync_clk_ref,clk_ref,clk_ro,rstb;
wire ngtv_clk_ro,temp_q_prime,q_prime;

assign ngtv_clk_ro = ~(clk_ro);

d_flip_flop dff1(.Q(temp_q_prime),.D(clk_ref),.CLK(ngtv_clk_ro),.rstb(rstb));
d_flip_flop dff2(.Q(q_prime),.D(sync_clk_ref),.CLK(temp_q_prime),.rstb(rstb));
d_flip_flop dff3(.Q(error_ref),.D(q_prime),.CLK(ck_loop_dly),.rstb(rstb));

endmodule
```

Appendix A7. Verilog code of the TDC Top Module

```
`timescale 1ns / 1fs
module tdc_with_errcr(tdc_phase_error,clk_ref,clk_div,rstb,clk_loop,freq_lock);
input clk_ref,clk_div,rstb;
wire signed [13:0] temp_tdc_phase_error;
output signed [13:0] tdc_phase_error;
output clk_loop;
output freq_lock;
wire  sync_clk_ref,sync_clk_div;
wire [30:0] ro_phases;
wire [30:0] Qresults_for_clk_ref;
wire [30:0] temp_Qresults_for_clk_ref;
wire [30:0] Qresults_for_clk_div;
wire [30:0] temp_Qresults_for_clk_div;
wire [6:0]  fine_distance_for_clk_ref;
wire [6:0]  fine_distance_for_clk_div;
wire [7:0]  count;
wire [7:0]  count_clk_ref;
wire [7:0]  temp_count_clk_ref;
wire [7:0]  temp_count_clk_div;
wire [7:0]  count_clk_div;
wire [13:0] phase_error_coarse;
wire [13:0] phase_error_fine;
wire error_ref;
```

```
wire error_div;
wire clk_loop_dly;
wire t1u,t2d;
// RING OSCILLATOR AND REFERENCE PHASE DETERMINATION
ring_osc_31ph ro1 (.clk(ro_phases),.rstb(rstb));
assign clk_ro = ro_phases[0];
// ERROR CONTROLLER
error_controller_ref
errref(.error_ref(error_ref),.ck_loop_dly(clk_loop_dly),.sync_clk_ref(sync_clk_ref),.clk
_ref(clk_ref),.clk_ro(clk_ro),.rstb(rstb));
error_controller_div
errdiv(.error_div(error_div),.ck_loop_dly(clk_loop_dly),.sync_clk_div(sync_clk_div),.c
lk_div(clk_div),.clk_ro(clk_ro),.rstb(rstb));
// SYNCHRONIZATION
synchronization sycref(.d(clk_ref),.q(sync_clk_ref),.clk(ro_phases[0]),.rstb(rstb));
synchronization sycdiv(.d(clk_div),.q(sync_clk_div),.clk(ro_phases[0]),.rstb(rstb));
// LOOP CLOCK GENERATION
phase_frequency_detector
pfd(.t1u(t1u),.t2d(t2d),.ck_loop(clk_loop),.ck_ref(clk_ref),.ck_div(clk_div),.rstb(rstb));
frequency_lock
fld(.freq_lock(freq_lock),.t1u(t1u),.t2d(t2d),.clk_ref(clk_ref),.clk_div(clk_div),.rstb(rstb
)) ;
assign #(0.5)clk_loop_dly = clk_loop;
// HAMMING RESULTS (FINE) (INCLUDING CLK_LOOP)
d_flip_flop_registers_31
dfref1(.Q(temp_Qresults_for_clk_ref),.D(ro_phases),.CLK(clk_ref),.rstb(rstb));
d_flip_flop_registers_31
dfref2(.Q(Qresults_for_clk_ref),.D(temp_Qresults_for_clk_ref),.CLK(clk_loop),.rstb(rs
tb));
d_flip_flop_registers_31
dfdiv1(.Q(temp_Qresults_for_clk_div),.D(ro_phases),.CLK(clk_div),.rstb(rstb));
d_flip_flop_registers_31
dfdiv2(.Q(Qresults_for_clk_div),.D(temp_Qresults_for_clk_div),.CLK(clk_loop),.rstb(r
stb));
hamming_with_error28
hd1(.distance(fine_distance_for_clk_ref),.phase(Qresults_for_clk_ref),.errc1(error_ref))
;
hamming_with_error28
hd2(.distance(fine_distance_for_clk_div),.phase(Qresults_for_clk_div),.errc1(error_div)
);
// COUNTER RESULTS AND FLIPFLOPS (COARSE) (INCLUDING
CLK_LOOP_DLY)
counter_8b_sequential cs1(.count(count),.clk(clk_ro),.rstb(rstb));
d_flip_flop_registers_8
dcref1(.Q(temp_count_clk_ref),.D(count),.CLK(sync_clk_ref),.rstb(rstb));
d_flip_flop_registers_8
dcref2(.Q(count_clk_ref),.D(temp_count_clk_ref),.CLK(clk_loop_dly),.rstb(rstb));
d_flip_flop_registers_8
dcdiv1(.Q(temp_count_clk_div),.D(count),.CLK(sync_clk_div),.rstb(rstb));
d_flip_flop_registers_8
```

```
dcdiv2(.Q(count_clk_div),.D(temp_count_clk_div),.CLK(clk_loop_dly),.rstb(rstb));
// TRANSFORMATIONS
manual_transformation_block_v9
mtbv9(.hd1(fine_distance_for_clk_ref),.hd2(fine_distance_for_clk_div),.coarse1(count_
clk_ref),.coarse2(count_clk_div),.manually_signed_fine_distance(phase_error_fine),.ne
w_coarse_distance(phase_error_coarse));
// FINAL RESULT
fulladderv2
fd2(.in1(phase_error_fine),.in2(phase_error_coarse),.out(temp_tdc_phase_error));
assign #(0.6) tdc_phase_error = temp_tdc_phase_error;
endmodule
```

CURRICULUM VITAE

Name Surname : Tamer EREN

EDUCATION:

B.Sc. : 2019, Istanbul Medipol University, School of Engineering and Natural Sciences, Biomedical Engineering

B.Sc. (Double Major) : 2020, Istanbul Medipol University, School of Engineering and Natural Sciences, Electrical and Electronics Engineering

PROFESSIONAL EXPERIENCE AND REWARDS:

- Internships = ASELSAN, TAI, Tübitak, Siemens
- 2015-2016 Fall Semester, High Honorary Student, Istanbul Medipol University
- 2015-2016 Spring Semester, High Honorary Student, Istanbul Medipol University
- 2016-2017 Fall Semester, High Honorary Student, Istanbul Medipol University
- 2016-2017 Spring Semester, High Honorary Student, Istanbul Medipol University
- 2017-2018 Fall Semester, High Honorary Student, Istanbul Medipol University
- 2017-2018 Spring Semester, High Honorary Student, Istanbul Medipol University
- 2018-2019 Fall Semester, High Honorary Student, Istanbul Medipol University
- 2018-2019 Spring Semester, High Honorary Student, Istanbul Medipol University
- 2019-2020 Fall Semester, High Honorary Student, Istanbul Medipol University
- 2019-2020 Spring Semester, High Honorary Student, Istanbul Medipol University

PUBLICATIONS, PRESENTATIONS, AND PATENTS ON THE THESIS:

- T. Eren, Z. N. Oktay, H. Doğan, and H. Ş. Savcı, "6 GHz Low Noise Amplifier design with 65nm CMOS for 5G/6G Applications," in 2020 12th International Conference on Electrical and Electronics Engineering, ELECO 2020, Nov. 2020, pp. 88–92, doi: 10.1109/ELECO51834.2020.00021.

A HIGH-RESOLUTION TIME TO DIGITAL CONVERTER DESIGN FOR ALL DIGITAL PHASE- LOCKED LOOPS

ORIGINALITY REPORT

9%	7%	4%	2%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS

PRIMARY SOURCES

1	Submitted to Eastern Mediterranean University Student Paper	1%
2	repository.tudelft.nl Internet Source	<1%
3	en.wikipedia.org Internet Source	<1%
4	Ahmed Elkholy, Tejasvi Anand, Woo-Seok Choi, Amr Elshazly, Pavan Kumar Hanumolu. "A 3.7 mW Low-Noise Wide-Bandwidth 4.5 GHz Digital Fractional-N PLL Using Time Amplifier-Based TDC", IEEE Journal of Solid-State Circuits, 2015 Publication	<1%
5	hdl.handle.net Internet Source	<1%
6	repository.ntu.edu.sg Internet Source	<1%
7	dr.ntu.edu.sg	