

# A Highly Linear Wide-Band Tunable Lna for Military Radio Applications

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## ABSTRACT

A wide-band tunable Low-Noise Amplifier (LNA) was designed to be used in military radios. The LNA works in the frequency range of 30–512 MHz where military walkie-talkies operate. To cover the wide range of operating frequencies, the output of amplifier is divided into four sub-bands with four separate external inductors and integrated capacitor arrays. The first part of the study analyzes the performance parameters such as the gain, tuning, matching, noise figure, and distortion. Layout of the design was completed, and post-layout simulations, including the layout parasitic effects, were run to quantify the performance. The LNA achieves a minimum of 12-dB gain across the entire operating frequency range. The minimum rejections achieved by the LNA at 10% and 20% offset from the center-tuned frequency were 7 dB and 13 dB, respectively. The LNA achieves a worst-case noise figure of 4.6 dB, and the impedance-match parameter ( $S_{11}$ ) is better than  $-20$  dB under all the conditions. The worst cases P1dB (1-dB Compression Point) and IIP3 (3rd Order Input Intercept Point) were 9.1 dBm and 18 dBm, respectively, across frequency and process-voltage-temperature corners. The design dissipates 20 mA from a 3.3-V power supply and uses a 1.5-V power supply for capacitor array termination.

**Keywords:** Tunable LNA, military radio, wide-band LNA, cascode amplifier, IIP3

## Introduction

Professional personal and military radios that are used for tactical communication between various vehicles, military units and combatants have been around since before the World War I. There has been a steady improvement on the technology ever since. Until recently, these radios have mostly been used for simple voice communication across vast distances. With the developments in wireless technologies, these radios also incorporated video and other data links in addition to audio communications. All these advancements result in more rigorous specifications for the design of these radios, ranging from higher sensitivity requirements to greater resilience to blockers.

The usage scenarios for such equipment place various system requirements on the designer. Professional and military radios usually have multiple types, ranging from hand-held walkie-talkies to vehicle radios. While hand-held units have output power in the 30+dBm range, vehicle units can output as high as 45+dBm. This becomes a major concern when a hand-held unit is nearby a vehicle unit, since the high power transmitted by the vehicle unit will act as a blocker and de-sensitize the hand-held unit carried by the personnel. The signal power reaching the Low Noise Amplifier (LNA) input in this scenario can be as high as  $-10$ dBm. This requires careful filtering of the undesired signals by the receiver in order not to degrade performance. Since these wide-band systems have very high ratio between the highest channel frequency (512MHz for this design) and lowest channel frequency (30MHz), it becomes very cumbersome to design a tunable filter that can tune in the whole range. Owing to the very low bottommost channel frequency, integration of such filters is extremely burdensome due to large component values. As a result, these types of high performance radios are designed and built using discrete filters and amplifiers.

Since each of these filters and amplifiers can only cover limited number of frequency bands, multiple of these are used in parallel and switched in and out of operation depending on the operation band. Having large number of discrete components to design a system increases the complexity of a viable solution. Moreover, volume and power dissipation of the system, which are critical metrics, especially

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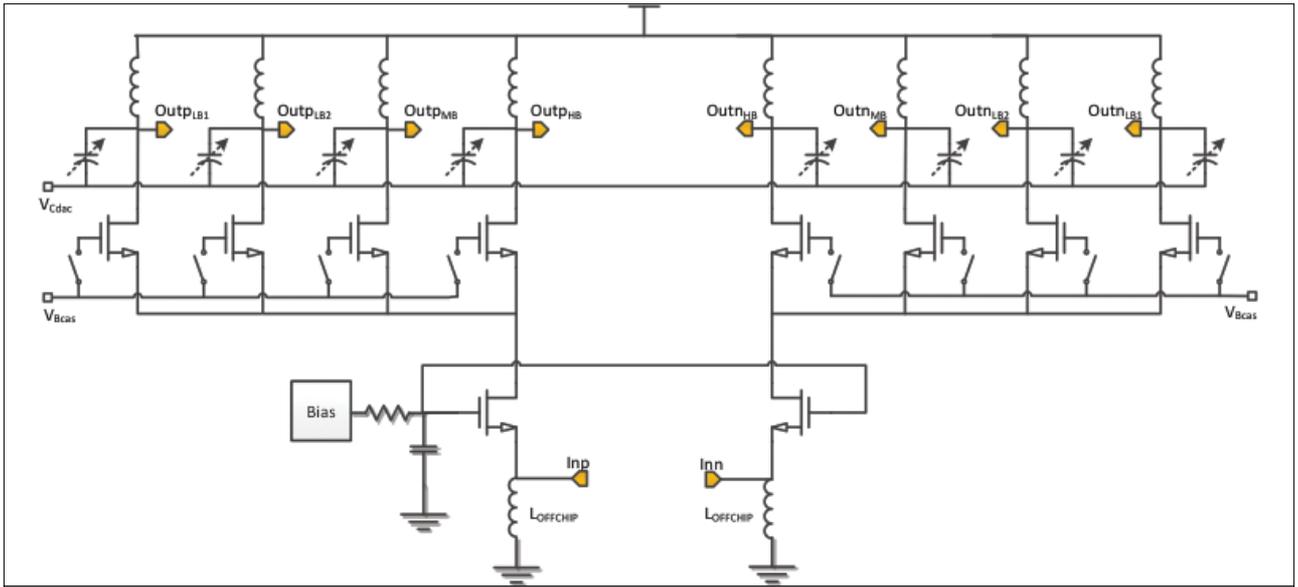
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**Figure 1.** Transistor level schematic for the tunable wide-band LNA

for mobile military units, increase accordingly. This necessitates a drive towards higher integration to reduce size and power.

Although there are not many examples of amplifiers for such applications in the literature, various wide-band amplifiers exist that are aimed for Cable TV systems that works in the frequency range of 50-850MHz [1-3]. These amplifiers use standard design approaches with high power dissipation for linearity. Other solutions utilize feedback to linearize the wide-band amplifiers for better linearity [3-5]. Other solutions utilize noise cancellation to reduce noise in wide-band amplifiers [6].

In this work, we designed a tunable wide-band LNA that is suitable for use in professional civil and military radios. In order to meet the sensitivity goal of  $-120\text{dBm}$  for a 25KHz voice channel in the system it will be used, Noise Figure (NF) of the amplifier needs to be less than 5dB for a quadrature receiver with 8dB minimum SNR (Signal-to-Noise Ratio). Minimum gain of the amplifier will be limited to around 12dB at the center frequency and consequently blocker power will be kept near constant by rejecting the signal at 20% offset by around 12dB. In order for the system not to saturate with  $-10\text{dBm}$  blocker at 20% offset frequency and resolve  $-120\text{dBm}$  channels, the amplifier needs to have a 1dB compression point in access of  $0\text{dBm}$ . Accordingly, while the desired signal at the output is amplified, the blocker power will be constant. Same LNA can be cascaded various times to realize a distributed type receiver where the blocker is kept at a level that doesn't overload the circuitry. Owing to relatively low top channel frequency of 512MHz, the design was realized using a well-established technology of 180nm CMOS from United Manufacturing Corporation (UMC). Metal-Insulator-Metal (MIM) capacitors were used due to their lower parasitic bottom plate capacitance which becomes extremely important when tuning in a wide range [7].

The organization of this paper is as follows. Part II gives design analysis and equations. Part III shows the simulation results and gives performance metrics for the design. Part IV summarizes work and gives conclusion remarks.

### Design Analysis

The tough requirements for distortion performance of the LNA necessitates the employment of all the possible design methodologies to reduce distortion. The foremost is to use a differential approach to nullify the second order harmonic and intermodulation distortion terms since in such wide band systems, second order terms fall in band for most of the input channels. The only second order distortion terms generated in differential design is due to mismatch between the differential signal paths, which can be minimized with careful layout and calibration.

A differential cascode amplifier with the output divided into four sub-bands with four cascode branches is designed. The four outputs are connected back to a single node for the next stage input via a switch network and AC coupling capacitors. The top level schematic and the multiplexing network at the output of the design is given in Figure 1, 2 respectively and the subsections below discusses the design metrics.

### Input Impedance Matching

In order to prevent reflections and maximize the power transfer from the antenna to the input of the amplifier, it needs to match to  $50\Omega$  differentially. Wide-band operation frequency of the amplifier limits the types of input topologies that can be used. Feedback has been used to achieve wide-band matching in some prior art [3-5], however this increases the complexity of the design, stability across frequency needs to be ensured and Noise Figure increases due to the feedback network. Additionally, feedback

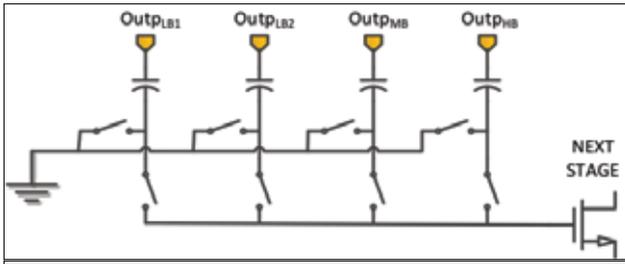


Figure 2. Output multiplexing network

creates a direct path from output to the input, which causes Local-Oscillator (LO) leakage into the antenna to increase. In order to mitigate these issues, a common gate amplifier is used to ensure matching in the whole frequency range.

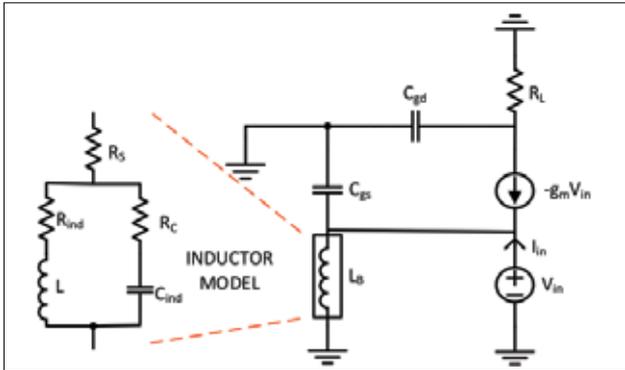


Figure 3. Small signal schematic of a common gate amplifier with off-chip inductor model

Figure 3 shows the single-ended input small signal network for the amplifier. This model can be used to calculate the input impedance equation using Kirchoff's Current Law (KCL) at the input node. The inductor used is an off-chip inductor selected from the Coilcraft products [8]. The main purpose of this inductor is to create a very low resistance bias path for the amplifier so that the transistors can be biased. This inductor is chosen to give a much higher impedance in the frequency range of 30-512MHz compared to 25 ohms single-ended so that the input signal flows into the input devices rather than into the inductor. The inductance value chosen is around 780nH, which corresponds to an impedance value of  $j170\Omega$ . Self-resonant frequency of the inductor is close to 600MHz, which is beyond the input frequency range of our system.

Inductor model given in Figure 3 is used to simulate the amplifier. However, for deriving the input impedance equation, only  $R_{ind}$  and  $C_{ind}$  which are the dominant components are used for the sake of simplicity. Writing KCL equations, input impedance can be found to be:

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{g_m + s(C_{gs} + C_{ind}) + 1/(R_{ind} + sL)} \quad (1)$$

where  $g_m$ ,  $C_{gs}$  and  $C_{gd}$  are the transconductance, gate-source capacitance and gate-drain capacitance for the transistor.  $R_L$  represents the resistance seen at the drain of the input device.

For the design values of the  $C_{gs}$ ,  $C_{ind}$ ,  $R_{ind}$  and  $L$ , equation (1) approximates to  $1/g_m$  in the frequency range of interest. This enables the designer to set the  $g_m$  value equal to 40mS for a near perfect matching at the input.

### Gain and Output Tuning

As mentioned above, the very high dynamic-range requirements of these receivers require adequate filtering of the undesired signals. Employing larger order filters increases the selectivity of the amplifier at the cost of increased complexity, power and cost. Furthermore, resistive and capacitive parasitics in the circuit places a theoretical limit to the selectivity that can be achieved with a single amplifier. Because of these reasons, a simple tunable inductor-capacitor (LC) network is employed at the output of the amplifier to achieve at least 10dB rejection at 20% offset frequency from the received channel. The center frequency of a parallel LC tank circuit is given by [9,10]:

$$\omega_s = \frac{1}{\sqrt{LC}} \quad (2)$$

Equation (2) shows that in order to tune the output center frequency from 30MHz to 512MHz with a given inductor value, the capacitor value needs to change  $(\omega_2/\omega_1)^2 = (512/30)^2$  times. This ratio is equal to 291, hence it is not possible to tune capacitors or varactors in such a wide range. Therefore, the output of the design is divided into 4 sub-bands in order to reduce the tuning range of the output capacitors. The four sub-bands that are used in the design are 30-50MHz, 50-100MHz, 100-200MHz and 200-512MHz. The highest tuning range for the sub-bands is for the high band and it is equal to  $(512/200)^2 = 6.55$  times.

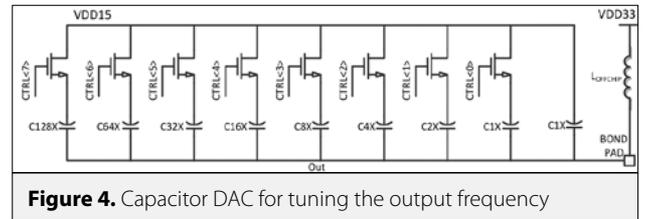
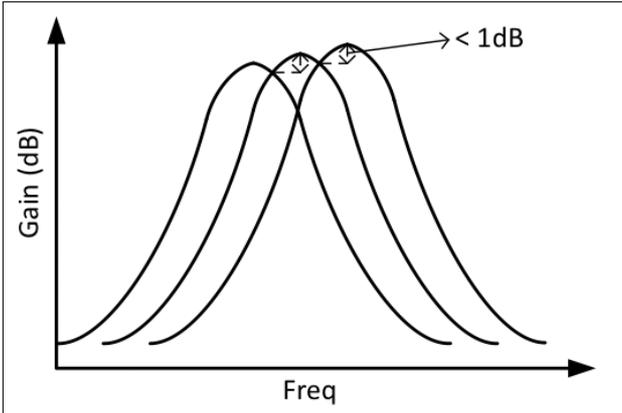
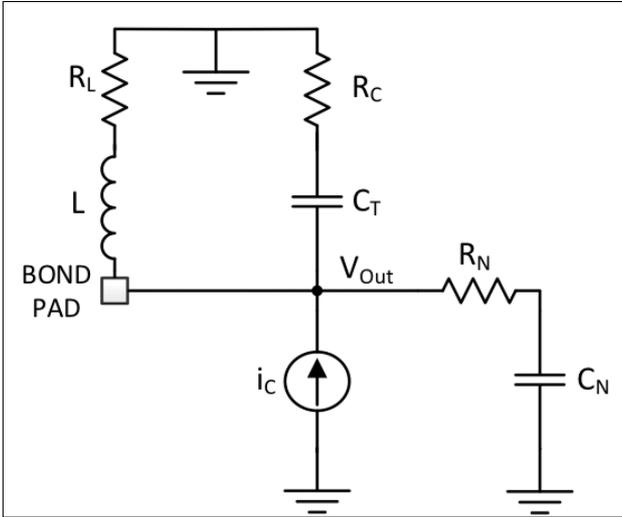


Figure 4. Capacitor DAC for tuning the output frequency

Figure 4 shows the capacitor array for each of the positive and negative output nodes. A binary weighted capacitor array is used to cover the frequency range of each of the four sub-bands. In order to maximize the capacitance density of the array, high density thin-oxide core MOS capacitors are used as long as the total parasitic capacitor permits. In order to comply with the reliability requirements of these devices, 1.8V lower than the gate drive voltage needs to be applied to the bottom plate terminal. This corresponds to 1.5V since the output of the amplifier has 3.3V DC through the load inductor, hence a DC supply of this value was used to terminate the bottom plate side of the capacitor. The use of 1.5V also enables the use of core devices as array switches, which is advantageous due to the reduces turn-on resistance and parasitic capacitance. Each time the array setting is incremented or decremented by one, the center frequency of the LC filter jumps up or down. The Least-Significant-Bit (LSB) of the array was chosen to give less than 1dB roll-off from the



**Figure 5.** Gain vs. Frequency for different tuning settings of the amplifier



**Figure 6.** Schematic for the equivalent output load network.

center gain to the intersections of the gain curves for two subsequent tuning settings as shown in Figure 5.

Figure 6 shows the equivalent output impedance network for one of the output branches. The signal current from the cascode node is given by  $i_c$  and flows into the output impedance to generate the output voltage.  $L$  is the external inductor used for tuning at the output node and  $C_T$  is the equivalent total capacitance at the output.  $R_L$  and  $R_C$  denote the series resistances with the inductor and the capacitor respectively.  $R_L$  is composed of metal sheet resistance and  $R_C$  is composed of resistances of the switches in the capacitance array in addition to metal sheet resistances. These resistances have a big impact on reducing the quality factor ( $Q$ ) of the output load network, hence they need to be minimized.  $C_N$  and  $R_N$  are the equivalent load capacitance due to the next stage and the series resistance due to signal routing traces and intrinsic gate resistances respectively.

In order to find the equivalent output network impedance, we can write KCL at the output node and derive  $Z_{Out} = V_{Out}/i_c$ . This analysis gives the output admittance to be:

$$Y_{Out} = \frac{1}{sL+R_L} + \frac{sC_T}{1+sC_T R_C} + \frac{sC_N}{1+sC_N R_N} \quad (3)$$

This equation is the most general form for the equivalent output admittance and it is difficult to get any insight from it.  $C_N$  is the gate capacitance for the next stage and is usually much smaller than  $C_T$  in the network.  $R_N$  is mostly the routing resistance and can be comparable or smaller than  $R_C$  since the latter is composed of routing and switch resistances. For the sake of simplicity, we can assume that the  $R_N$ - $C_N$  network will be much smaller than the  $R_C$ - $C_T$  branch, hence can be ignored. We then can write the equation for the output impedance as:

$$Z_{Out} = \frac{R_L+s(L+C_T R_C R_L)+s^2 L C_T R_C}{1+sC_T(R_C+R_L)+s^2 L C_T} \quad (4)$$

And the gain of the amplifier is given by:

$$A_V \cong g_m Z_{Out} \quad (5)$$

It is apparent from equation (4) that the network resonates at the frequency given in (2), where  $s^2$  term is equal to  $-1/LC_T$ . When  $R_L$  and  $R_C$  values are close to each other and  $L$  is much larger than  $C_T R_C R_L$  term, output impedance simplifies to:

$$Z_{Out} \cong \frac{L}{C_T(R_C+R_L)} \quad (6)$$

As expected, this equation suggests that for increasing  $R_C$  and  $R_L$  values, the equivalent load impedance goes down. Furthermore, a minimum  $L/C_T$  ratio has to be kept to ensure that the amplifier has the minimum required gain. This is another reason to divide up the whole frequency range to 4 sub-bands since a large tuning range for the capacitor increases its value to a range that may be comparable to  $L$  value. Figure 6 shows how the impedance of the load network varies for varying  $R_L$  and  $R_C$  values using the actual design values for  $L$  and  $C_T$ . It is apparent that as the  $R_L$  and  $R_C$  values increase a lot more than  $1 \Omega$  range, the output impedance scales down considerably. This has two consequences; the gain of the amplifier goes down and the rejection for blockers offset from the center frequency is reduced. It is apparent from the figure that even with  $1 \Omega$  series resistance with the inductor and capacitor, the rejection at 20% offset is around 10 dB, which is what we aim in this design. Consequently, layout techniques to reduce the series resistance with the external inductor and integrated capacitor array is very critical and are employed in this design.

### Noise Figure

During operation, the amplifier is configured as a cascode amplifier working in one of the sub-bands mentioned in Part 2.2 above. Consequently, input referred noise of the amplifier will be that of a differential cascode amplifier and is given by [9, 10]:

$$\frac{v_{in}^2}{\Delta f} = 8kT \left[ \frac{\gamma}{g_m} + \frac{(1+g_m R_S/2)^2}{R_L g_m^2} \right] \quad (7)$$

where  $k$  is the Boltzman's constant,  $\gamma$  is a technology dependent scaling factor for the process used,  $R_L$  is the equivalent load resistance at the center frequency of the output tank and

$R_s$  is the source resistances. Using (7), noise figure of the amplifier can be calculated to be:

$$NF = 1 + \frac{2\gamma}{g_m R_s} + \frac{2R_s}{R_L} \left[ \frac{1+g_m R_s/2}{R_s g_m} \right]^2 \quad (8)$$

A perfect differential matching at the input of the amplifier requires that  $1/g_m = R_s/2$ . Using (11), we can show that the equation simplifies to [10]:

$$NF = 1 + \gamma + \frac{2R_s}{R_L} \quad (9)$$

Equation (9) shows that the only way to control the NF of the amplifier is by increasing the gain by using a higher Q inductor. Otherwise, the NF is limited by the technology coefficients. Since the most important goal of this amplifier is to achieve higher filtering at the output by utilizing high-Q off-chip inductors, the design automatically minimizes the NF.

### Distortion Analysis

In wide band receivers, linearity of the design blocks are extremely important due to the fact that there is a wide range

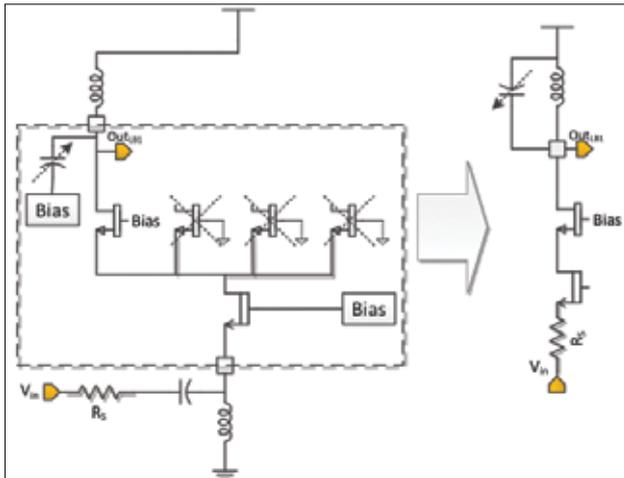


Figure 7. Schematic of half-circuit for distortion calculations

of incident frequencies that overload the system. As explained in the introduction, the specific system this amplifier is designed for may have a blocker of -10dBm at 20% offset when trying to receive a -120dBm desired signal and our design needs to be able to handle this power in full gain mode.

In order to understand the distortion performance of the amplifier designed, we can coarsely analyze it for linearity. Since the design is pseudo-differential, we can take half of the circuit and solve for distortion and the result will be the same for the differential amplifier for the fundamental tone and the odd harmonics. Even harmonics at the two outputs will be in phase and will cancel each other. One of the sub-bands of the amplifier will be on at a given time, so the equivalent circuit for distortion analysis reduces to the one on the right in Figure 7. At the frequencies of interest, the cascode device acts as an ideal current buffer, therefore doesn't introduce considerable distortion. Furthermore, for the sake of simplicity, we will assume that the programmable capacitor array at the output is biased at deep inversion, hence small-signal at the output doesn't cause considerable capacitance variation, which causes distortion. With these assumptions, the distortion of the single-ended amplifier is equal to that of a common gate amplifier with a source resistance. With Taylor Series expansion, the differential drain current of the amplifier can be written as [11]:

$$I_o = a_1 V_i + a_2 V_i^2 + a_3 V_i^3 \dots \quad (10)$$

$$a_1 = \frac{g_m}{1+g_m R_s} \quad (11)$$

$$a_2 = 0 \quad (12)$$

$$a_3 = -\frac{2(\frac{\mu C_{ox} W}{2L})^2 R_s}{(1+g_m R_s)^5} \quad (13)$$

where  $\mu$  is the mobility of electrons,  $C_{ox}$  is the gate capacitance density and  $W/L$  is the gate-to-length ratio of the input transistors. It is apparent from Eq. (15) that for a fully matched amplifier, the second order distortion term is zero. Eq. (13) suggests that in order to minimize the third order distortion,  $W/L$  ratio needs to be minimized,

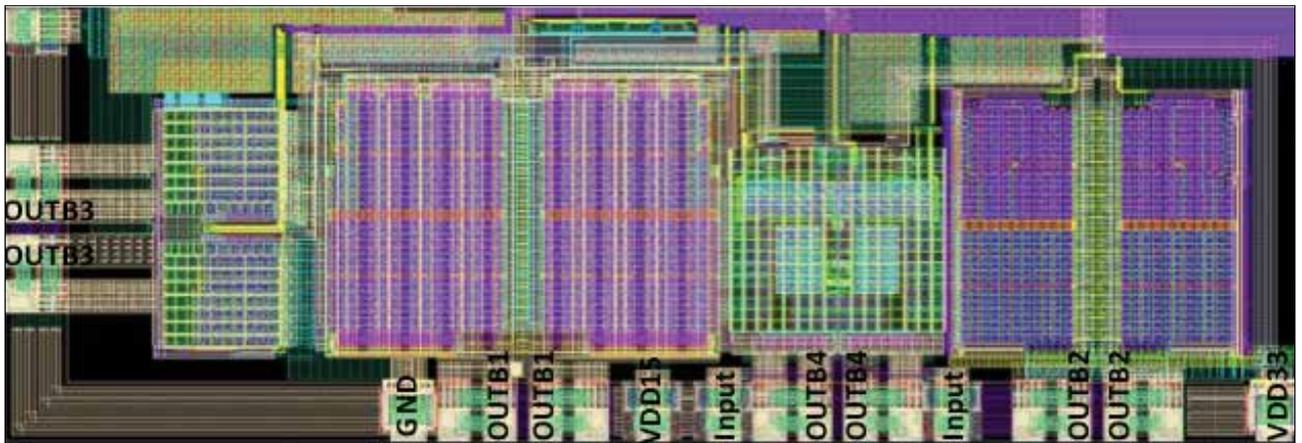


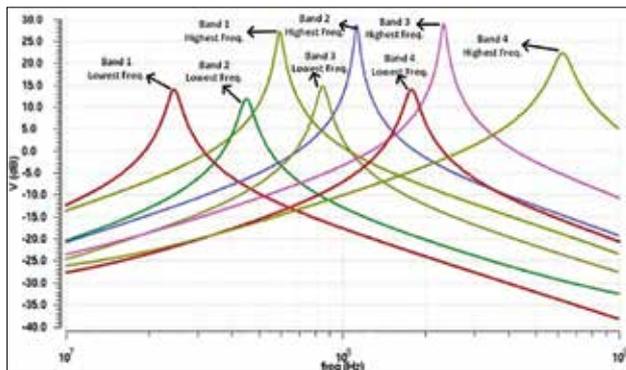
Figure 8. Layout of the wide-band LNA

while maximizing the  $g_m$  of the input device. Transconductance ( $g_m$ ) of the input device is already decided on from Eq. (1) in order to have a adequate matching at the input port. Therefore, in order to minimize W/L ratio for a given  $g_m$  value,  $V_{GS} - V_{TH}$  (also called  $V_{DSAT}$ ) of the input device needs to be maximized. Additionally, careful design steps need to be taken to minimize the distortion due to secondary effects such as Channel Length Modulation. For this, the designer needs to make sure that the  $V_{DS}$  is maximized for all the transistors.

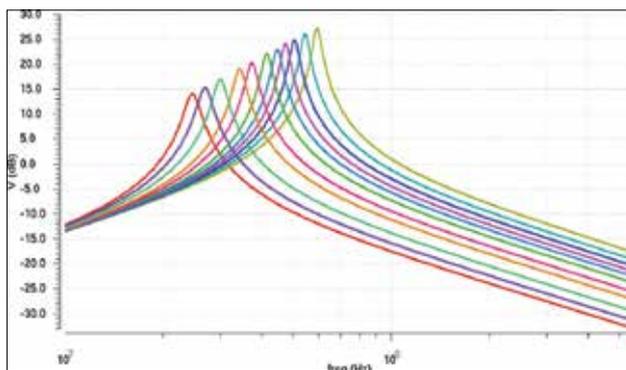
The amplifier was designed in 0.18 $\mu$ m standard CMOS process and layout was optimized to minimize parasitic resistors that limits the Q of the inductors. For this purpose, two pads for each output node was used to double-bond the outputs to the package pins and reduce series resistor. This can be seen in the layout of the design in Figure 8. This figure shows the four subbands, the bonding pads for these, the input pads and the pads for supply and ground connections. The design occupies an area of 2200 $\mu$ m-by-700 $\mu$ m without the bonding pads and 2500 $\mu$ m-by-850 $\mu$ m with the bonding pads.

**Table 1.** Design Parameters

BAND	RS ( $\Omega$ )	RC ( $\Omega$ )	K	L-ind (nH)	Cind (fF)
30-50MHz	20	10m	165 $\mu$	81	56
50-100MHz	23	10m	72.2 $\mu$	35.7	59
100-200MHz	13	50m	48 $\mu$	21.9	54
200-512MHz	9	13m	32 $\mu$	12	58



**Figure 9.** Minimum and maximum tuning for each band



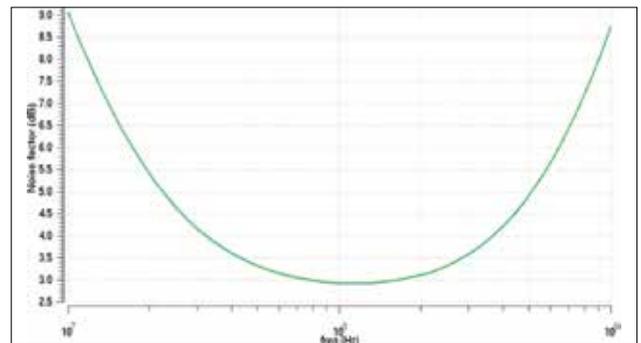
**Figure 10.** Minimum and maximum tuning for each band

## Simulation Results

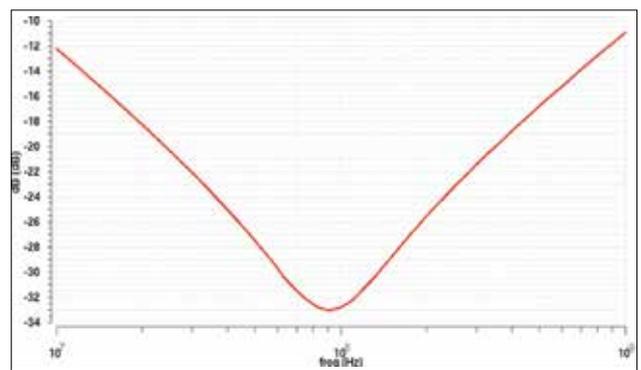
The design was verified across Process-Voltage-Temperature (PVT) using Cadence Spectre simulations. Post layout simulations were also performed to estimate the degradation in performance due to layout, bondwire and external inductor parasitics. The design works from 3.3V and 1.5V supplies for power supply and capacitor array terminations respectively, and consumes 20mA from the 3.3V supply.

Figure 3 shows the inductor model used to model the external inductors [12] and Table 1 shows the values and the coefficients for the inductors from Coilcraft.

Figure 9, 10 shows the gain and tuning curves for the amplifier. Figure 8 shows the lowest tuned frequency and highest tuned frequency for each of the sub-bands given in Table 1. Each band has overlap with the neighboring band at high and low ends of the range to make sure that there are no gaps in tuning in the whole frequency range of interest. The gain of the amplifier ranges from a minimum of 12dB to a maximum of 28dB across the whole band of 30-512MHz. This gain increase happens since the Q of the output tank increases as a function of frequency as we tune it higher within a sub-band. An attenuator following the amplifier can be used to limit the overall gain to a lower value in the case of high input power. Figure 9 shows how the amplifier tunes in the first sub-band of 30-50MHz by showing sample tuning settings that ranges from 0 to 255. Each sub-band has a total of 255 tuning steps as a result of 8 bit tuning control.



**Figure 11.** Noise Figure vs. Frequency for the high-end tuning of the 30-50MHz sub-band



**Figure 12.** S11 vs. Frequency across the whole band

**Table 2.** Performance results

Band (MHz)	Freq (MHz)	NF (dB)	S11 (dB)	%10 offset rejection (dB)	%20 offset rejection (dB)	P1dB at 20% offset (dBm)	In-Band IIP3 (dBm)
30-50	30	4.6	-21	10	16.5	9.1	18
	50	3.4	-26	12	18.5	11	21
50-100	50	3.9	-26.5	11.2	17.5	9.8	21
	100	2.9	-33	15.6	22.1	13	21
100-200	100	3.3	-33.7	13.2	19.6	9.6	21
	200	2.8	-33	16.7	23.2	9.2	21
200-512	200	3.6	-31	9.9	16	9.5	21
	512	3.3	-21	7	12.8	9.2	21

NF: noise figure; P1dB: 1-dB compression point; IIP3: 3rd order input intercept point

Figure 11 shows the Noise Figure of the amplifier when the output is tuned to the high end of the 30-50MHz sub-band. As the amplifier is tuned to different frequencies, the frequency where the minimum NF is achieved moves with the center frequency. Table 2 shows the NF at the low and high ends of each sub-band. Worst case NF is 4.6dB across the whole frequency range.

Figure 12 shows the simulated impedance-match parameter (S11) result for the amplifier and it is less than -20dB across the whole frequency range of 30-512MHz. Table 2 gives S11 results at the low and high ends of each sub-band. The rejection of undesired signals at 10% and 20% frequency offset, which is one of the critical specifications for the design, are also given in Table 2. These rejection amounts are adequate to reject the incoming undesired signal enough to keep it under control at the output of the amplifier. The worst case 1dB compression point ( $P_{1dB}$ ) and the third order input intercept point (IIP3) for the amplifier are 9.1dBm and 18dBm, respectively, across the whole band as given in Table 2.

## Conclusion

In this paper, we have presented a wide-band tunable LNA that has been designed in 0.18 $\mu$ m CMOS process from UMC. The design has been laid-out and post layout simulations were run to include the parasitic effects. The design dissipates 66mW from a 3.3V supply to meet the tough requirements of military radios. In the first part of the paper, the proposed design has been analyzed for gain, tuning, matching, noise figure and distortion. The LNA works in the frequency range of 30-512MHz and achieves a minimum gain of 12dB across the whole range. Worst case Noise Figure was simulated to be 4.6dB and S11 is less than -20dB across

frequency and PVT. The design is highly linear and achieves a minimum of 9.1dBm  $P_{1dB}$  and 18dBm IIP3 in worst case settings.

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