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A 12-bit, 100 kS/s, PVT robust SAR ADC in 65 nm CMOS process

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ABSTRACT

We present a highly robust 12-bit, 100 kS/s Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) that excels in mitigating the effects of mismatch, temperature variations and process corners. A modified hybrid switching method is developed in design of the Capacitive Digital-to-Analog Converter (C-DAC) that saves 17 % of the DAC power consumption. Furthermore, we utilize a switched local feedback loop in the pre-amplifier circuit of the comparator that significantly minimizes the offset. Using this technique, the 3-sigma offset is reduced from 11.33 mV to 0.37 mV. Moreover, a high performance latched-based Bit Slice Unit (BSU) is proposed to preserve the successive codes during each conversion. Designed in 65 nm CMOS technology, the ADC operates in −55 °C to +125 °C temperature range, consuming only 1.55 μW with a 0.7V supply voltage and occupying a 0.6 mm^2 area.

1. Introduction

With evolution of CMOS technology, Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs) can go well above several hundred MS/s and still provide outstanding energy-efficiency. Among the building blocks of a SAR ADC, the capacitive DAC used to consume a significant portion of the total power, primarily influenced by the switching scheme and the total capacitance of the capacitor array which is usually used as a sampling capacitor in a top plate sampling structure. Thanks to technology scaling, using small unit capacitors with C_u as small as 0.25 fF, sampling capacitance has decreased to 280 fF for a 10-bit 80 kHz ADC [1]. However, noise and matching requirements complicate the design of ADCs with more than 10bits using such small unit capacitors. For reduction of switching energy, various switching schemes have been proposed to improve the power efficiency [1–5]. The monotonic scheme saves up to 81 % of the average energy compared with the conventional method [3]. The average switching energies in widely used DAC switching schemes of conventional scheme, the monotonic scheme, the V_{CM}-based scheme, the switching-back scheme, and merged capacitor switching (MCS) scheme in a 10-bit ADC are $1363.3CV^2_{REF}$, $255.5CV^2_{REF}$, $170.2CV^2_{REF}$, $127.5CV^2_{REF}$ and $84.7CV^2_{REF}$, respectively. In addition to the decreased switching energy, the area of the DAC is greatly reduced as well. For instance, the DAC area in the monotonic scheme is almost halved compared to the conventional switching method [3]. Other advanced and novel switching techniques exist that significantly reduce the DAC switching power. Nevertheless, they encounter challenges such as increased complexity in the digital section [6], susceptibility to reference voltages [7], and no area reduction compared to the conventional scheme [8]. Overall, the enhancements to DAC switching schemes have led to other blocks' power consumption, particularly the comparator, becoming nearly comparable to the ADC's overall power consumption.

In this paper, we employ a hybrid switching algorithm for design of the DAC, as outlined in Ref. [2], which significantly reduces switching energy to $15.8CV^2_{REF}$, resulting in an average reduction of 93.8 % compared to the widely monotonic scheme. Furthermore, it showcases a substantial area-saving benefit, up to 50 % compared to its monotonic counterpart. Nonetheless, this approach encounters reset energy nearly double its switching energy, totaling $31.2CV^2_{REF}$. To mitigate this issue, we introduce a refined resetting technique, resulting in a 17 % decrease in the overall DAC energy consumption. In addition, we propose a robust Bit Slice Unit (BSU) circuit, that significantly enhances the resilience of the ADC to variations in Process, Voltage, and Temperature (PVT). Furthermore, a locally calibrated pre-amplifier circuit is presented to effectively minimize the offset of the comparator at the initiation of the conversion cycle. The rest of the paper is organized as follows. In Section II, a brief summary of the conventional hybrid switching scheme is provided, followed by the presentation of the proposed reset-efficient algorithm. Section III discusses the structure of the proposed SAR ADC, and its building. The ADC's performance is covered in Section IV,

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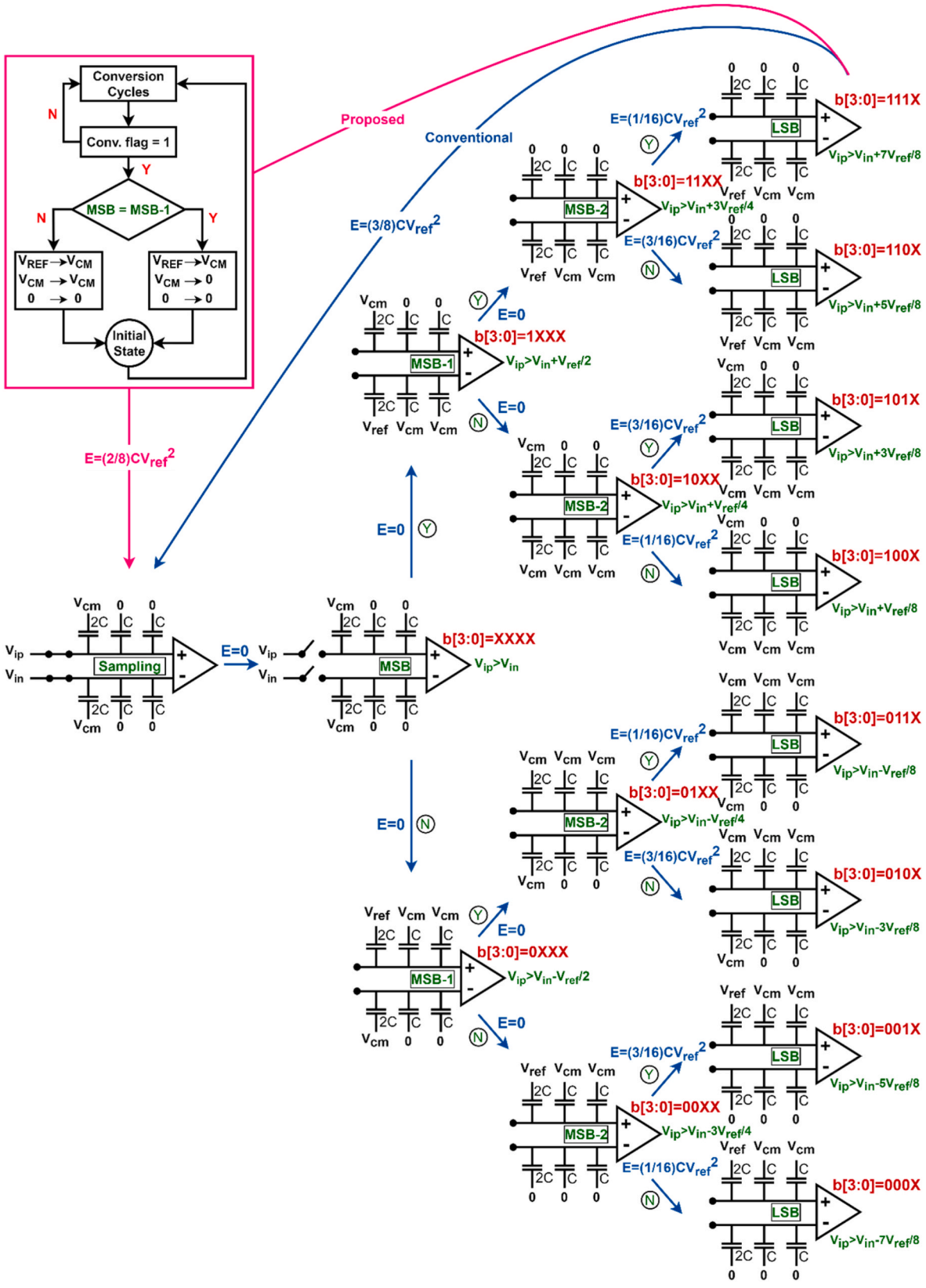

Fig. 1. Hybrid switching scheme in a 4-bit DAC.

and Section V concludes the paper.

2. DAC switching scheme

- *Conventional Hybrid Method:*

The conventional binary-weighted hybrid switching scheme for a 4-bit DAC is illustrated in Fig. 1. In the sampling phase, the bottom-plates of the capacitors are initially loaded with the sequence of [V_{CM}, 0, 0, …], where V_{CM}=V_{REF}/2. Simultaneously, the top plates sample the differential inputs V_{IP} and V_{IN}. During the conversion phase, the top plates of the capacitors are disconnected from the inputs, and with the first rising edge of the comparator clock, the initial comparison is performed directly and the MSB bit is obtained with zero switching energy. If $V_{IP} > V_{IN}$, MSB equals '1'. In this case, the voltage on all capacitors at the positive side remains unchanged, while the voltage on the negative side increases by V_{CM} (by switching V_{CM} to V_{REF} and GND to V_{CM}). Conversely, if $V_{IP} < V_{IN}$, MSB equals '0', and the capacitors at the negative side remain unchanged, while the voltage on the positive side increases by V_{CM} in the same manner. Since the voltage on the bottom-plates of the capacitors increases by the same value, here V_{CM}, the DAC consumes "zero" energy to move to the next state.

When the second comparison cycle is triggered, the MSB-1 bit is determined. In case $V_{IP} > V_{in}$, MSB-1 equals '1' and the voltage on the positive side drops down by V_{CM}. As a result, the voltage on positive side decreases by V_{REF}/4 for the next comparison. The same procedure occurs if $V_{IP} < V_{IN}$. Upon the third rising edge of the comparator, the MSB-2 bit is derived again with no energy consumed. From this state onward, the voltage on the bottom plate of the next-right capacitor increases by V_{CM}, in response to the preceding output bit, and the DAC begins to consume energy. With the next rising edge of the comparator, the last bit (LSB) is attained, and the DAC returns to the sampling phase while consuming $(3/8)CV_{REF}^2$ energy, which is twice the energy consumed in all previous cycles combined [2]. The efficiency of this scheme lies in the fact that, in a conventional binary-weighted SAR ADCs, the DAC uses roughly 87.5 % of its switching energy to detect the first three bits. Thanks to the lack of energy consumption during the initial three comparison cycles in the hybrid switching, this scheme demonstrates remarkable energy efficiency, outperforming many existing schemes. Another attractive benefit of the hybrid DAC switching method is its greatly reduced area. As depicted in Fig. 1, with only 4-unit capacitors in total, a 4-bit ADC is achieved. This translates to a 50 % and 75 % reduction in area compared to the monotonic and the conventional scheme.

- *Modified Reset-Efficient Method:*

The issue of reset energy in the conventional hybrid scheme arises from the necessity to load the bottom plates of the capacitors with the sequence [V_{CM}, 0, 0, …] in every cycle. Considering the resetting path depicted in Fig. 1, when the DAC is reset to the initial state, the energy drawn from the V_{CM} reference is

$$(3/8)CV_{REF}^2 \tag{1}$$

This value is constant over all possible output codes [2].

In the proposed resetting path depicted in Fig. 1, the DAC capacitors are not immediately loaded with that sequence. Instead, they first enter an intermediate state where the capacitors are charged based on the state of the MSB and MSB-1 bits. On the next rising edge of the clock, they subsequently transition to the initial state of [V_{CM}, 0, 0, …]. When the conversion flag equals '1', signifying the completion of the conversion for one sampled data, the following steps occur.

1. If MSB equals MSB-1, then any V_{REF} on the bottom plates of any capacitor, both on the positive and negative sides, drops down to V_{CM}, and all others are reset to ground.
2. If MSB is not equal to MSB-1, then V_{REF} drops down to V_{CM}, and the voltage on bottom-plates of other capacitors remain unchanged.

Following these steps, the DAC enters its initial state. Schematically illustrated in Fig. 2, where the output code assumes 110X, since MSB and MSB-1 are equal, the initial action is for V_{REF} to drop down by V_{CM}, while all other capacitors are connected to ground. Afterwards, the subsequent sampling phase will take place. This way, the energy drawn from the DAC is

$$E_{r1} = -2CV_{CM}\left(\frac{V_{CM}}{2} - V_{CM} - \left(\frac{3V_{REF}}{4} - V_{REF}\right)\right) = 0 \tag{2}$$

$$E_{r2} = -2CV_{CM}\left(\frac{V_{CM}}{2} - V_{CM} - 0\right) = CV_{CM}^2 \tag{3}$$

$$E_{rt} = E_{r1} + E_{r2} = CV_{CM}^2 = (2/8)CV_{REF}^2 \tag{4}$$

Comparing equation (4) with equation (1), a 33.3 % reduction in reset energy is achieved through this transition. To ensure a fair comparison with the original hybrid scheme [2], the behavioral simulation

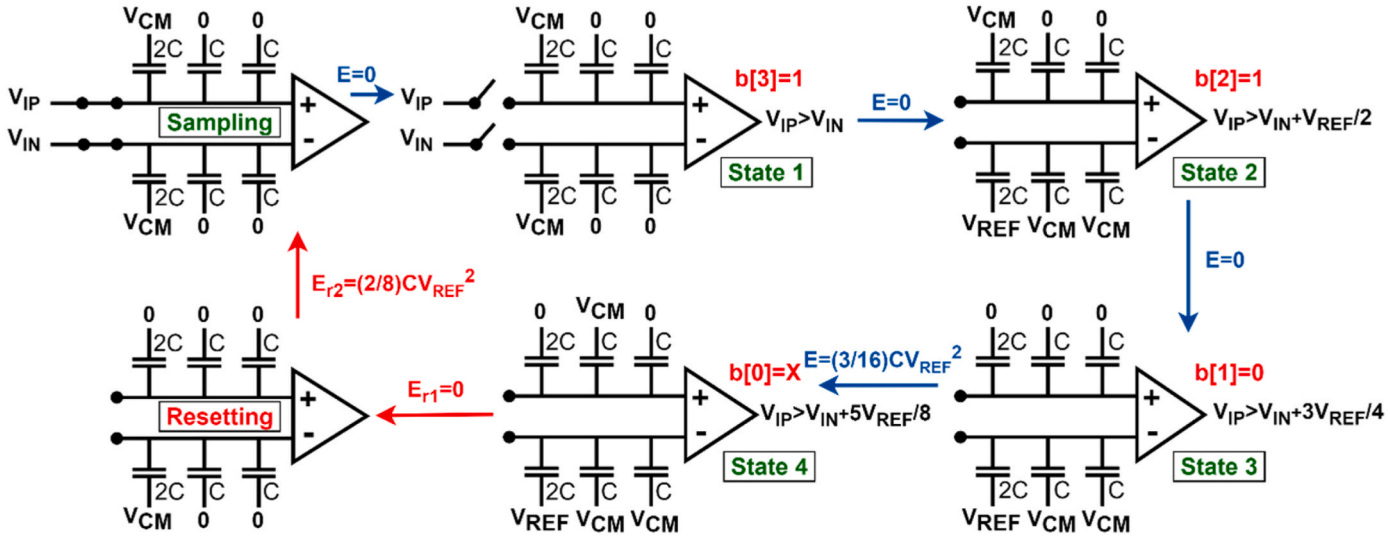

Fig. 2. Reset-Efficient Switching Method when the output is 110X

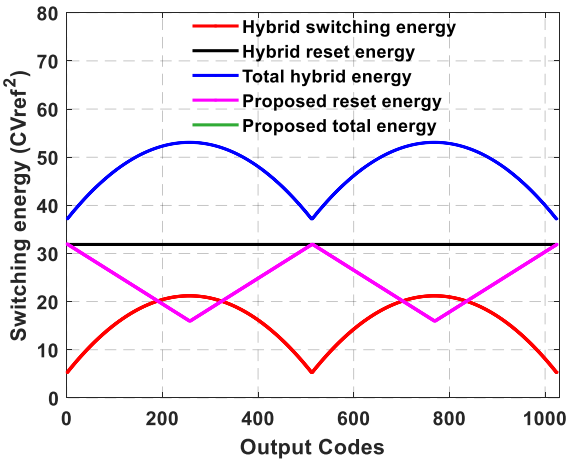

Fig. 3. Switching energy consumption of the conventional and the proposed algorithms in 10-bit ADC.

Table 1
Performance summary of the DAC switching schemes in 10-bit ADC.

Switching Method	Avg. Energy (CV^2_{REF})	Avg. Reset Energy	Reset Energy Saving (from V_{CM})	Tot. Energy (CV^2_{REF})	Tot. Energy Saving
Hybrid [2]	15.8	31.2	Reference	47	Reference
Proposed	15.8	23.2	26 %	39	17 %

of the proposed reset-efficient switching scheme is carried out in MATLAB, considering a 10-bit DAC. As shown in Fig. 3, the reset energy in the proposed method varies across the complete range of output codes and maintains an average lower than that of [2]. The effectiveness of the proposed reset switching method on the DAC's overall energy consumption is further evident in Table 1. In ultra-low power design, V_{CM} reference voltage is usually generated using a voltage divider [4]. Due to the current drawn from the V_{CM} reference, this voltage can exhibit variations. It is crucial to ensure the average voltage deviation remains below one LSB for optimal performance. In the proposed method, the average energy drawn from V_{CM} decreases by 26 %, facilitating the design of the V_{CM} generator.

3. Proposed SAR ADC

The proposed synchronous SAR ADC with the efficient resetting technique is presented in Fig. 4(a) with the timing waveforms in Fig. 4 (b). The input signal passes through a network comprising a 50Ω resistor, a 1 nH inductor, and a 2 pF capacitor. The internal resistance of 50Ω is utilized to prevent rapid changes at the input. The 1 nH inductor simulates wire bonding, while the 2 pF capacitor represents ESD parasitic effects [9,10]. For a 12-bit and 100 kS/s ADC, an external clock with a frequency of 1.3 MHz governs the sampling and conversion processes. Upon the rising edge of the clock, the input signal is sampled on the capacitive DACs (C-DAC), which also serve as the sampling capacitors, through bootstrapped switches. The sampling phase, lasting one clock cycle, is initiated at intervals of 10 μsec? Simultaneously, the inputs of the comparator are disconnected from the DACs, and the comparator undergoes calibration over a duration equivalent to the sampling phase (770 nsec). Subsequent clock cycle reconnects the comparator inputs to the DACs, concluding the sampling phase. In the meantime, the sampled data undergoes comparison, and MSB is obtained. To ensure proper functionality, slight delays are introduced in the sampling and the comparator clocking signal. With each rising edge of the comparator clock, the output bit is determined, initiating the SAR algorithm. The algorithm iteratively settles one of the DACs with a new voltage, progressively approaching the other one. This process continues until all 12 bits are obtained.

On the falling edge of the 12th comparator clock, the reset signal rst, associated with the signal Q in the last Bit Slice Unit (BSU_0), is activated and it lasts for half a cycle, ~385 nsec? Immediately after the activation of the rst signal, the DACs are pre-reset based on the states of the MSB and MSB-1. Following this, the sampling phase begins and the comparator undergoes calibration while disconnected from the DACs. This cyclic process of activation, resetting, and calibration continues consistently, in accordance with the predefined operational sequence. In our design, we adopt the bootstrapped switch of [11] and incorporate a stacked version from Ref. [12] to reduce leakage current. Following this, the building blocks of the ADC are analyzed as follows.

- *Bit-Slice-Unit (BSU)*

The outputs of the comparator, V^+ and V^-, are fed into Bit Slice Units (BSUs), and they are sequentially preserved in the latches until the end of one complete conversion. A conventional BSU circuit and its waveforms are shown in Fig. 5. Right before the start of conversion phase, the enable signal EN associated with BSU_{11} is set to zero, resulting in Q being equal to zero. Since the Q signal of any BSU serves as the EN for the subsequent BSU, it follows that all BSUs will be reset to ground. Consequently, both $bit^+[11:0]$ and $bit^-[11:0]$ will be maintained at low level.

When the enable signal (EN) of BSU_{11} transitions to 1, the conversion process begins. At the rising edge of the BSU clock (CLK), bit [7] is acquired based on the values of V_{OP} and V_{ON}, where V_{OP} and V_{ON} signify the comparison results obtained from the comparator. The BSU clock is triggered once V_{OP} and V_{ON} are settled, ensuring the reliable processing of the result. During the reset phase of the comparator, V_{OP} and V_{ON} are both pre-charged to V_{DD}. This action causes the CLK signal associated with all BSUs to go low through the NAND gate. Consequently, Q switches to 1, enabling the subsequent BSU. This sequential process continues until BSU_0 establishes bit [0] and resets the ADC. One primary limitation of the conventional BSU circuit in Fig. 5, is its sensitivity to PVT variations. As shown in Fig. 6(a), when the temperature rises, the internal node *n* experiences continuous charging toward V_{DD} due to the off-current in the path consists of the transistors M_7-M_8-M_{10}. Moreover, due to the fact that all BSUs share the same V_{OP} and V_{ON} signals of the comparator (see Fig. 4(a)), the values of V_{ON} and V_{OP} undergo changes during each conversion cycle. Thus, preceding BSUs must retain their respective outputs until the end of 12th conversion cycle. However, as depicted in Fig. 6(b), the conventional BSU demonstrates vulnerability to mismatches and is also sensitive to temperature variations.

The proposed BSU circuit is shown in Fig. 7(a). During the reset phase, Q_B is set to 1, and both internal nodes and outputs are grounded through S_0–S_3. When EN is equal to 1, at the rising edge of the CLK, Q_B transitions to zero, and M_7 connects the sources of M_9 and M_{10} to V_{DD}. Due to the latched structure of the proposed method, nodes n and p are immediately settled based on the values of V_{OP} and V_{ON}, determining the output voltages P and N. Apart from its faster operation compared to the conventional counterpart, the proposed circuit is more reliable in preserving output values. In scenarios where V_{OP} and V_{ON} change every cycle or the temperature rises, internal nodes n and p are effectively maintained with the assistance of transistors M_{P1}-M_{P3}. For instance, if the off-current in M_9 attempts to charge node n through M_{11}, the transistor M_{P2} provides a short resistance path to the ground, allowing the off-current of M_9 to flow through M_{P2} rather than M_{11}. This ensures the retention of node n. In addition, transistors M_{P3} and M_{P4} serve as an extra feedback path to enhance the preservation of internal nodes. Fig. 7 (b) shows the simulation results of the proposed circuit under various corners, temperatures, and in the presence of mismatch (using Cadence-Spectre with monte carlo analysis enabled). The results demonstrate the

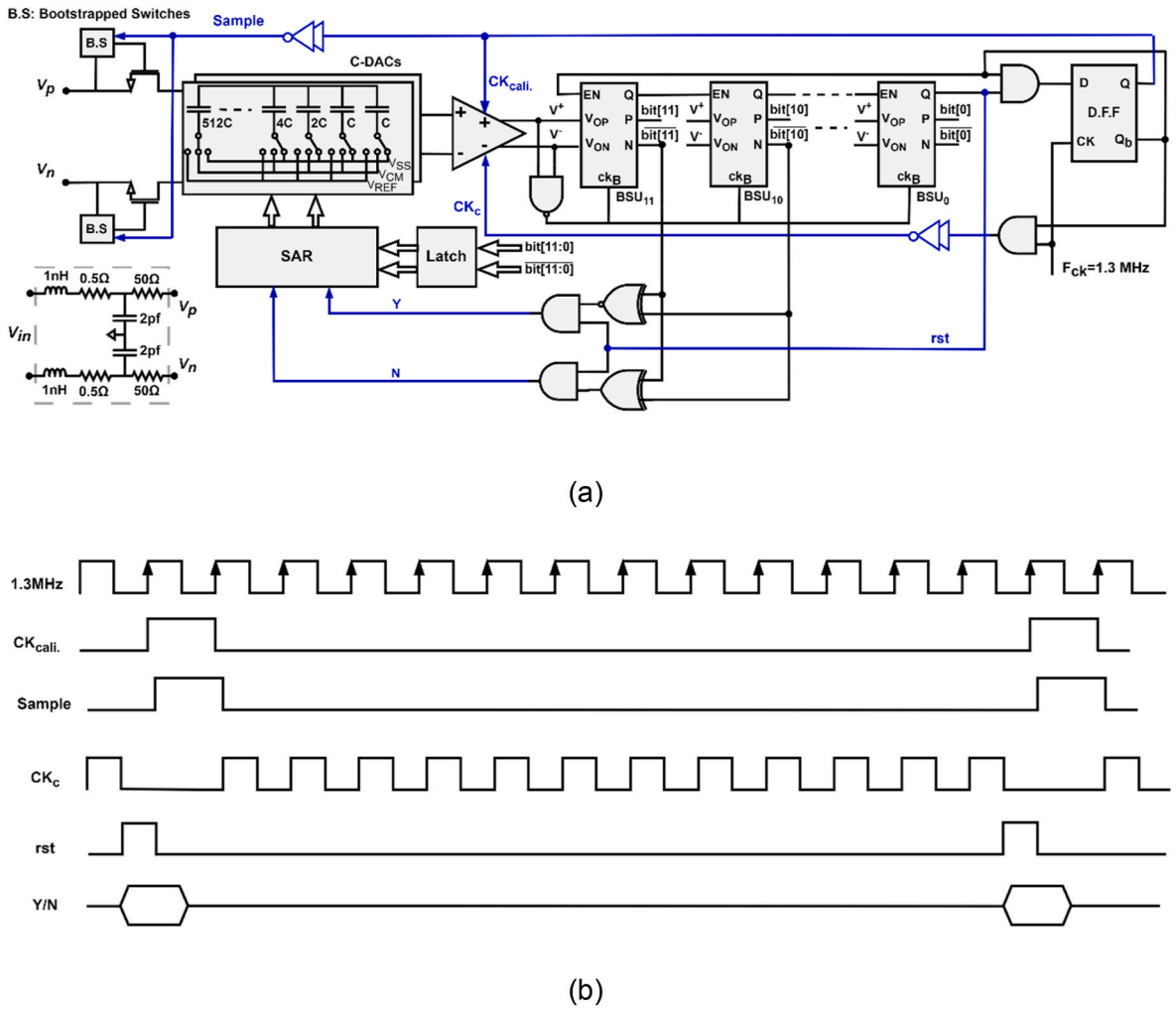

Fig. 4. (a) Proposed 12-bit SAR ADC and (b) its timing diagram.

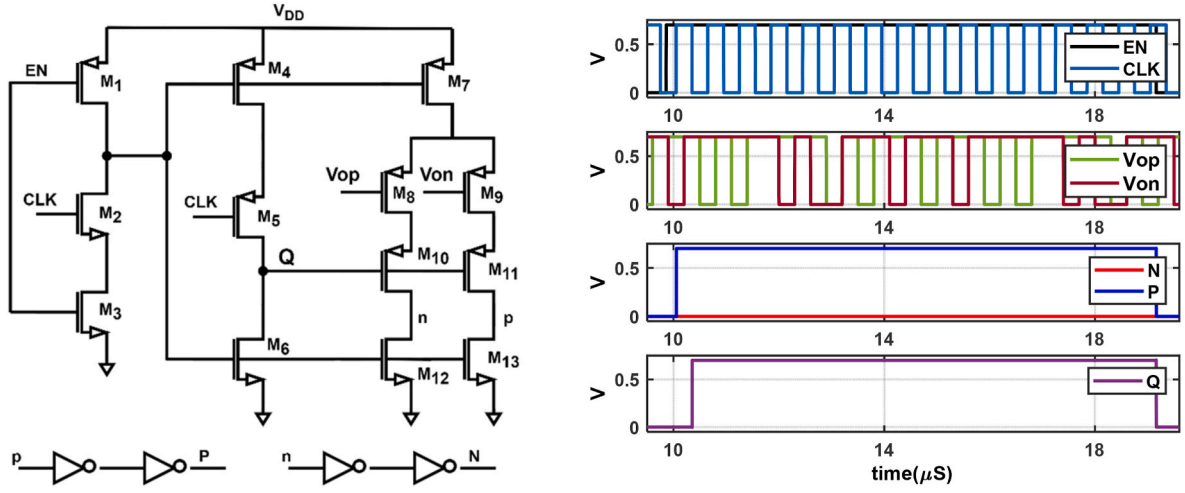

Fig. 5. Conventional BSU circuit and its waveforms.

superiority of the proposed BSU compared to the conventional one.

- *Comparator:*

The accuracy of the comparator in a SAR ADC is crucial for optimal ADC performance. While a conventional StrongArm Latch (SAL) is well-suited for ADCs with fewer than 10 bits, it encounters challenges, particularly in terms of common-mode offset and noise. A comprehensive study on StongArm Latches has been conducted in Ref. [13]. However, for ADCs requiring more than 10 bits, a single SAL may prove

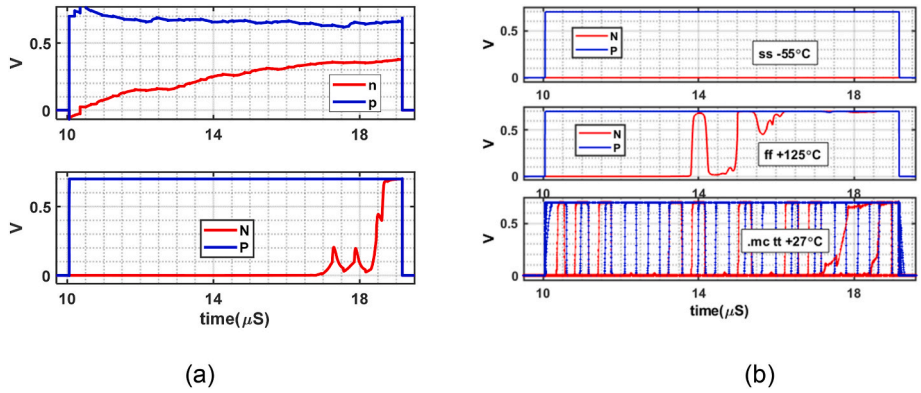

Fig. 6. Conventional BSU: (a) charge/discharge of internal nodes (b) variations in the presence of PVT.

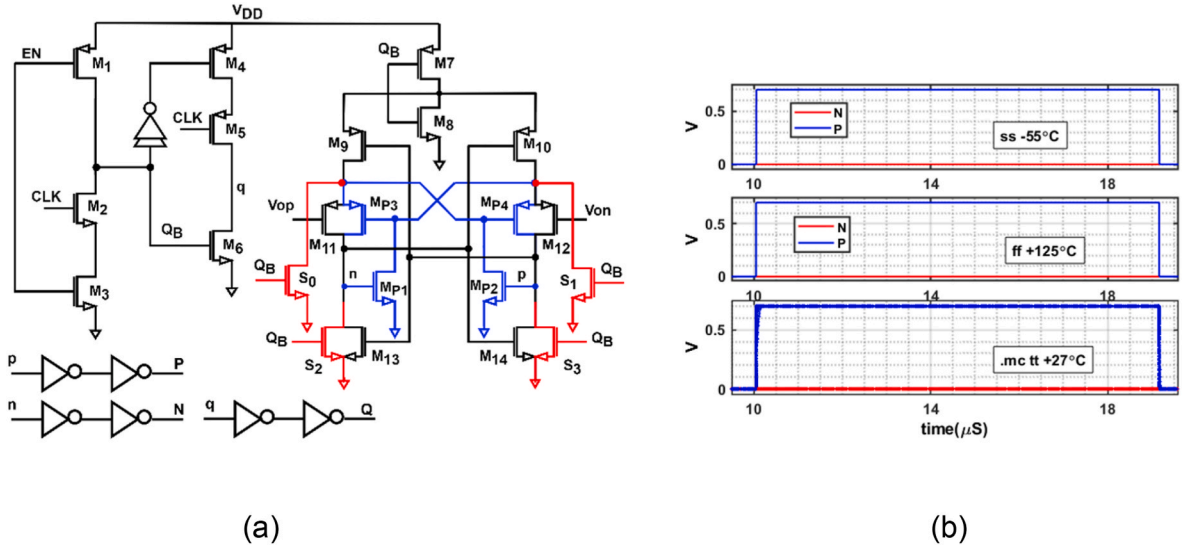

Fig. 7. (a) Proposed BSU circuit and (b) its waveforms in the presence of PVT variations.

insufficient. To address this, a common strategy involves employing a pre-amplifier followed by a SAL. This configuration mitigates non-linearity and noise in the SAL by leveraging the gain of the pre-amplifier, simplifying the overall design. On the other hand, in a low-voltage design, the pre-amplifier typically undergoes offset calibration to ensure a high dynamic range. The proposed comparator structure, shown in Fig. 8, integrates a calibrated static type pre-amplifier preceding a non-calibrated SAL. Its operation is as follows: During the calibration phase, the input transistors M_1 and M_2 are isolated from the inputs and connected to the common voltage V_{CM} through the calibration switches S_1–S_2. These switches are activated by $CK_{Cali.}$ signal illustrated in Fig. 4(b). Simultaneously, the current source I_{SS} flows through the signal path, involving transistors $M_{1\text{-}4}$ and the load resistors R. When the signal $CK_{Cali.}$ goes low, the switches S_3–S_4 are activated and any errors in the signal path are sampled on the capacitors C_c. Due to the low value of V_{CM} compared to the threshold voltage, transistors M_1-M_2 are forced to operate in weak inversion. Thus,

$$I_D = I_0 e^{\frac{V_{GS}-V_{th}}{V_T}}\left(1 - e^{-\frac{V_{DS}}{V_T}}\right) = \frac{I_{SS}}{2}, I_0 \propto \mu_n C_{ox}\frac{W}{L} \tag{5}$$

where V_T is the thermal voltage. Given the assumptions listed below, the offset voltage at the output of the pre-amplifier is calculated.

$$\begin{cases} V_{th1} = V_{th} + \frac{\Delta V_{th}}{2} \\ V_{th2} = V_{th} - \frac{\Delta V_{th}}{2} \end{cases} \quad \begin{cases} I_{01} = I_0 + \frac{\Delta I_0}{2} \\ I_{02} = I_0 - \frac{\Delta I_0}{2} \end{cases} \quad \begin{cases} R_1 = R\left(1 + \frac{\Delta R}{2}\right) \\ R_2 = R\left(1 - \frac{\Delta R}{2}\right) \end{cases} \tag{6}$$

The offset resulting from variations in the threshold voltage, V_{th}, and I_0 of the input transistors, as well as the mismatch due to the load resistors R is found using Eqs. (7)–(9), respectively. And, the total offset at the output is given by Eq. (10).

$$\Delta V_{out_{\Delta V_{TH}}} = R(I_{D1} - I_{D2}) = RI_0\left[e^{\frac{V_{GS}-V_{th}-\frac{\Delta V_{th}}{2}}{V_T}} - e^{\frac{V_{GS}-V_{th}+\frac{\Delta V_{th}}{2}}{V_T}}\right] \simeq -\frac{RI_{SS}\Delta V_{th}}{2V_T} \tag{7}$$

$$\Delta V_{out_{\Delta I_0}} = \Delta I_0 R e^{\frac{V_{GS}-V_{th}}{V_T}} \simeq \Delta I_0 R \tag{8}$$

$$\Delta V_{out_{\Delta R}} = \frac{I_{SS}}{2}\Delta R \tag{9}$$

$$\Delta V_{OUT}{}^2 = \left(\frac{RI_{SS}}{2}\right)^2\left[\left(\frac{V_{th}}{V_T}\right)^2\left(\frac{\Delta V_{th}}{V_{th}}\right)^2 + \left(\frac{\Delta I_0}{I_0}\right)^2 + \left(\frac{\Delta R}{R}\right)^2\right] \tag{10}$$

Equation (10) describes the overall output offset of the pre-amplifier during the calibration phase activation. As the calibration signal goes

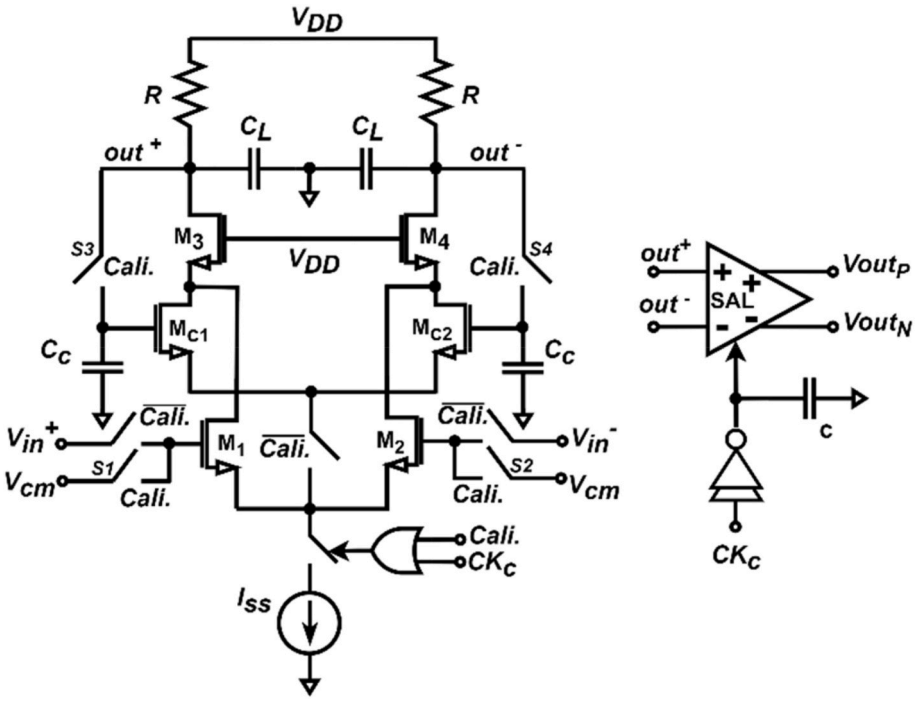

Fig. 8. Proposed comparator circuit.

low, M_1-M_2 reconnect to the inputs, and M_{C1}-M_{C2} pair is configured in parallel with the input transistors M_1-M_2. As a result, M_{C1} and M_{C2} draw currents in response to the offset voltage specified in Eq. (10), sampled on the capacitors C_C. This setup ensures an equal output voltage for each branch. Thus,

$$\Delta V_{out_{\Delta V_{OUT}}} = RI_c\left[e^{\frac{V_{GS}-V_{th}-\frac{\Delta V_{OUT}}{2}}{V_T}} - e^{\frac{V_{GS}-V_{th}+\frac{\Delta V_{OUT}}{2}}{V_T}}\right] \simeq -RI_c\frac{\Delta V_{OUT}}{V_T} \tag{11}$$

where I_c represents the current drawn from M_{C1}-M_{C2} pair. On the other hand, the sum of I_{c1} and I_1 should equal I_{SS} once the calibration phase is complete. This implies that I_{ss} in Eq. (10) is now a fraction of its previous value (denoted as $\alpha\Delta V_{OUT}$). To eliminate the offset, $\alpha\Delta V_{OUT}$ should be equivalent to Eq. (11). Given that I_1 is αI_{ss}, the value of I_c would be $(1-\alpha)I_{ss}$. So, we have,

$$\alpha \simeq \frac{(RI_{SS}/V_T)}{1+(RI_{SS}/V_T)} \tag{12}$$

In the preceding calculations, we disregarded the effect of mismatch in M_{C1}-M_{C2} pair. For the sake of simplifying the design, we set the current of M_{C1}-M_{C2} pair to be less than 10 % of the I_{SS} so that the mismatch in M_{C1}-M_{C2} is not a critical factor. Thus, we chose α to be 0.9. Using Eq. (12) and with $V_T \simeq 25$ mV, RI_{SS} is found to be 225 mV. In addition, long-channel devices are employed for M_{C1}-M_{C2} to decrease their offset and flicker noise. While the mismatch in load capacitors C_Ls is not highly critical in the first order, it often dictates the need for sufficient settling time. Moreover, C_L determines the noise limitations of the amplifier. The mismatch in the capacitors C_C is not crucial, as they simply retain the offset in calibration phase for one cycle period.

The Monte Carlo analysis of the proposed pre-amplifier is shown in

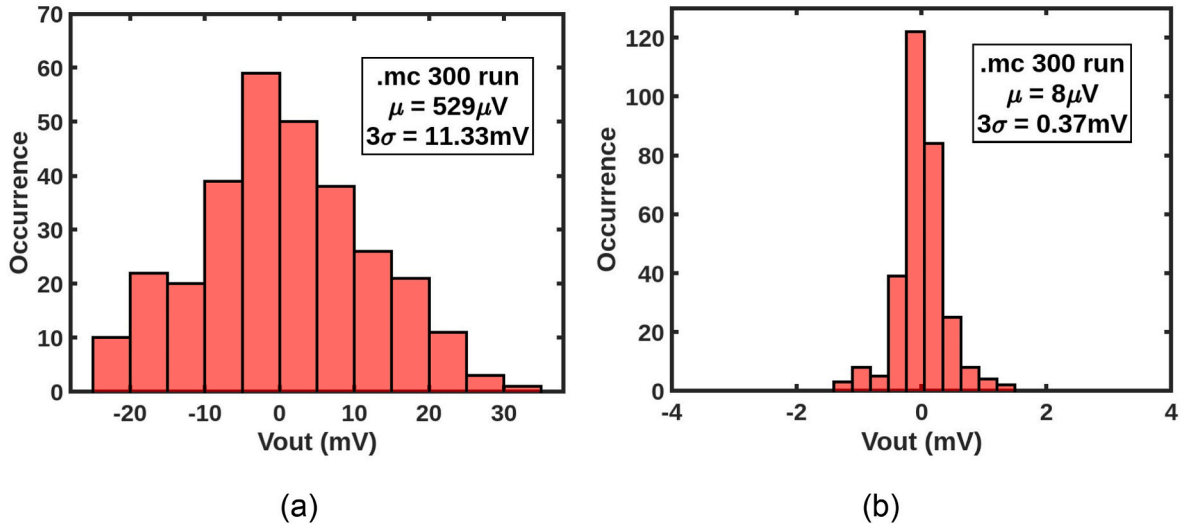

Fig. 9. MC analysis of the proposed pre-amplifier when calibration is (a) OFF and (b) ON.

Fig. 9 for $V_{OUT} = out^{+} - out^{-}$. The 3-sigma deviation of the pre-amplifier exhibits a substantial reduction from 11.3 mV to 370 μV when calibration is enabled, with mean values denoted by μ in both scenarios. In the hybrid switching method utilized in here, the input common-mode voltage varies from V_{CM} to $3/4V_{CM}$, ranging from 350 mV to 525 mV with V_{DD} of 700 mV. If a dynamic preamplifier were used, input common-mode voltage variations could indeed degrade linearity. However, the proposed preamplifier in Fig. 8, is of static type. Thus, remains highly unaffected by CM variations. Nevertheless, input common-mode variation tolerant technique described in Ref. [3] is applied during the design of both preamplifier and SAL to further mitigate any potential issues. The simulation results presenting the offset voltage versus input CM variation of the preamplifier is given in Fig. 10. The 3-sigma input offset of the preamplifier changes from 0.38 mV to 0.435 mV (55 μV change) during each comparison which is way smaller than the LSB size of 170 μV. Comparing with a fresh design, the comparator detailed in Ref. [14] achieves an offset with a mean value of −173μV and a 1-σ standard deviation of 0.562 mV, while consuming only a few nanowatts at a clock frequency of 100 kHz. In our proposed design, however, the comparator attains a very low mean value of 8 μV with a 3-σ standard deviation of 0.37 mV, while consuming less than 1 μW clocked at 1.3 MHz.

In addressing the noise, since the preamplifier stage serves as the dominant noise contributor, the input referred noise is mainly due to the followings.

1. Thermal noise of the load resistors R ($2 \times KT/C_L = 180$ μV) referred to the input by dividing it by the gain of the preamplifier, yielding 40 μV.
2. Thermal noise arising from input NMOS pair of the preamplifier, calculated as $\sqrt{2 \times \Delta f \times 4KT\gamma g_m^{-1}}$. With Δf = 650 kHz, γ ≃ 2 and $g_m = 24\mu A/V$, the thermal input referred noise due to the input NMOS pair of the preamplifier is 42 μV.
3. Flicker noise from the input NMOS pair of the preamplifier, calculated as $\sqrt{2 \times \Delta f \times K'/WLC_{ox}f}$. Through simulation, the input-referred noise due to the flicker noise of the input pair of the pre-amplifier is measured to be ~70 μV.

The noise sources from the SAL are neglected as they are divided by the square of the preamplifier gain. Summing up all noise sources with the $2 \times KT/C_S = 24$ μV noise of the sample and hold, the noise voltage at the input of the comparator totals 176 μV. Nearly half of the differential LSB size value, 340 μV. Comparing the proposed technique with novel techniques addressed in Ref. [15], namely majority voting and decreasing the noise bandwidth NBW, the proposed technique proves more suitable in the hybrid switching scheme. The study in Ref. [15] adopts a V_{CM}-based switching scheme to maintain offset voltage V_{OS} unchanged during the conversion period. Then, by increasing the number of votes, the input-referred noise (IRN) reduces. However, this technique results in an increase in comparison cycles, which in turn limits the ADC speed. Decreasing NBW is another straightforward technique to reduce noise power. To realize this [15], also allocates more time to determine the last bits. Since the required settling time of the CDAC tends to gradually reduce as the bit trials progress from the MSB bit to the LSB bit, some time are taken off from the DAC settling period to compensate T_{INT} (where $NBW = 0.5/T_{INT}$) in order to suppress IRN. However, this approach requires the ADC to be clocked asynchronously, and may prove inefficient in synchronous type ADCs.

4. Performance results

The SAR ADC is designed in the 65 nm CMOS process node with a sampling frequency of 100 kHz and V_{DD} as low as 0.7V. As mentioned earlier, the area of the capacitive DAC in the hybrid switching scheme is greatly reduced compared to its conventional counterpart by 75 %. This means that for a 12-bit ADC, only $1024C_u$ is needed to perform all 12 conversions [2]. Illustrated in Fig. 4(a), the MSB capacitor is only $512C_u$, compared to the monotonic scheme with $1024C_u$ and the conventional scheme with $2048C_u$ as the MSB capacitor [3]. Typically, due to the high value of the capacitive DAC, thermal noise is not a significant issue, leaving mismatch as the main source of non-linearity in the DAC design. In the 65 nm UMC process, the minimum value for a MOM-cap and MIM-cap is approximately 2.63 fF and 52 fF, respectively. MIM caps typically have excellent immunity to mismatch, while MOM caps are denser and smaller in area. To benefit from the precise matching characteristics of MIM capacitors, we employ an array of MIM capacitors in the capacitive DAC. Since, the minimum value for a MIM-cap is relatively large at approximately 52 fF, four MIM-caps are connected in series, resulting in an approximate unit cap value of 13 fF. Fig. 11 displays the 3-sigma error-bar plot of the SNDR of the designed ADC vs. unit capacitor with Monte Carlo analysis enabled. In the simulation, all other blocks were implemented by Verilog-A except the C-DAC. With an increased value in the MOM capacitor, the 3-sigma variation of the SNDR is reduced. However, with a MIM unit cap of 13 fF, SNDR is the highest, and its variation is the lowest. With the hybrid switching scheme, the sampling capacitor reaches nearly ~13.3 pF. Despite occupying a larger area, this ensures effective thermal noise suppression

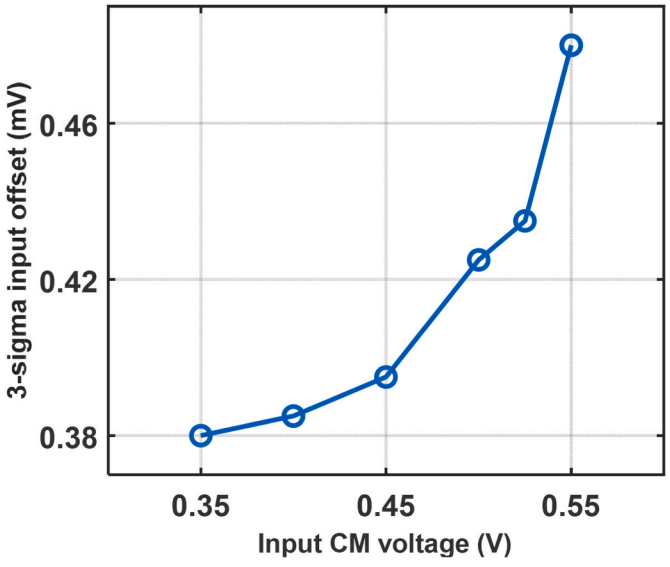

Fig. 10. Input common mode voltage vs the offset voltage.

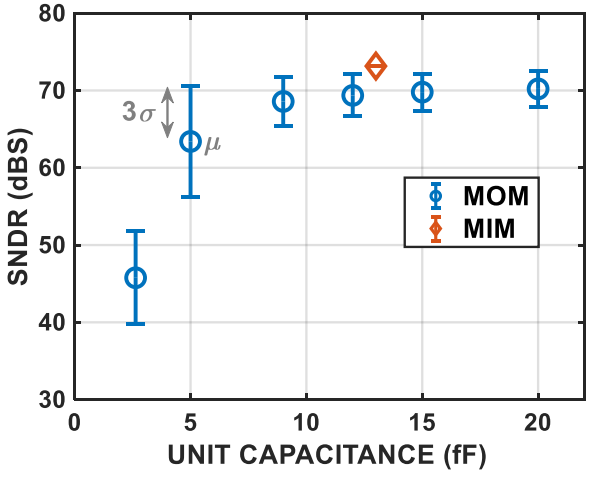

Fig. 11. SNDR vs. unit capacitor.

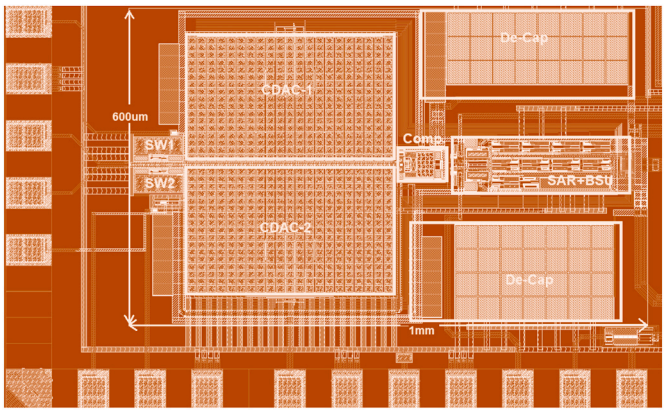

Fig. 12. Layout of the ADC

and also contributes to the elimination of clock feedthrough in the bootstrapped switches [11]. All of these factors contribute to a better SNDR.

The layout of the ADC is shown in Fig. 12. Two large decoupling capacitors are used to effectively cancel out the perturbations on the reference voltages. Excluding the de-caps, C-DACs occupy the largest area. The total resistance seen from the sampling capacitor is the series combination of the bootstrapped switch resistance, a constant 50Ω, and the resistance of the input signal source. It is crucial to maintain this resistance at a sufficiently low level to avoid impacting the settling time.

In an RC-based sample and hold circuit, the sampling period (t_S) should be much larger than the RC time constant. It follows $t_S \geq \ln 2^N$, where N is the number of bits. Fig. 13 represents the minimum sampling time needed for N bits resolution. For 12-bit accuracy, the sampling period needs to be at least 8.3 times the RC time constant to settle to 99.98 % of the input signal. This requirement dictates the value of the resistance R be less than 6kΩ, a condition that can be easily fulfilled. Fig. 14 displays the output FFT result of the ADC at both low and Nyquist input frequencies, and a family of curves in Fig. 15 depict the post-layout simulation results of the ADC under various corners within a temperature range of −55 °C to +125 °C, and nearly 10 % variation in supply voltages. The results in Figs. 14 and 15 were obtained with transient noise enabled by setting $f_{max} = 1$ GHz and $f_{min} = 200$Hz. V_{IN} is 320 mV sin-wave with common mode voltage of 350 mV. The reference voltage V_{REF} equals 0.7V as V_{DD}.

SAR ADCs are predominantly digital; thus, variations in V_{DD} and temperature have minimal impact on their functioning, particularly at

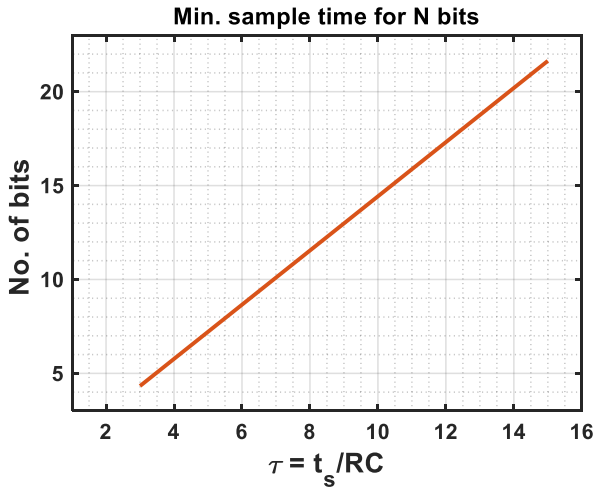

Fig. 13. Sampling time vs. number of bits achieved.

low speeds. Additionally, we developed a robust BSU that effectively handles PVT variations. Moreover, the preamplifier in the comparator is resistively loaded and biased with I_{SS}, resulting in a reasonable gain of approximately $G_{m1,2}R$ ($I_{SS}R/2V_T$). This gain is largely independent of the supply voltage at the first order and has sufficient gain across all corners and temperature ranges. As a result, the overall ADC shows promising performance.

DNL and INL are two important metrics that describe the performance of an ADC when dealing with non-linearity. In a well-designed ADC, both INL and DNL should be below 1-LSB. Fig. 16(a) presents the INL and DNL plots of the designed ADC. Thanks to the highly mismatch immune DAC structure and the low offset comparator design, DNL and INL are well below 1-LSB in magnitude, reaching the minimum and maximum values of −0.39/+0.22 for DNL and −0.36/+0.31 for INL. To further assess the ADC's resilience against mismatch, Fig. 16(b) illustrates the output code when the inputs are shorted to V_{CM}, and Monte-Carlo analysis is enabled with a 100-run. The common-mode voltage V_{CM} ($V_{REF}/2$) corresponds to the output code of 2048 in a 12-bit ADC. In the designed SAR ADC, the mean value is 2047, and in the case of mismatch, it deviates from its mean by less than 4 LSB. This mismatch is mostly due to the 3-sigma deviation we previously measured in the pre-amplifier, being 370 μV that is equivalent to around 2.2 LSBs. The results in Figs. 15 and 16 confirm the proposed ADC's high immunity to noise, distortion, and mismatch. Nevertheless, this advantage comes at the cost of a larger area.

The power consumption breakdown is shown in Fig. 17 for +27 °C and +125 °C in the typical-typical corner. In ambient temperature, the comparator consumes almost 60 % of the power. The SAR block occupies the smallest portion in the power consumption pie with 8 %. As the temperature increases, SAR corresponds to a significant portion, 42 %, while the comparator uses 26 % of the power. The performance of the proposed ADC is compared with other works in Table 2. While the comparator is automatically calibrated in every cycle to address mismatch, the substantial value of the unit capacitor eliminates the necessity for additional calibration in the C-DAC against mismatch.

The study in Ref. [17] showcases a resolution-reconfigurable dynamic zoom ADC achieving an impressive SNDR of 102.8 dB while consuming a mere 1.3 mW. Its input bandwidth remains constant at 20 kHz, with the input signal sampled at various rates to achieve different oversampling ratios (OSR). This ADC obtains the lowest figure of merit (FoM) at 287 fJ/step. Reference [20], despite having a lower SNDR and relatively higher FoM, presents a fully digital architecture that is particularly suited for increasingly scaled processes. In Ref. [16], a Noise-Shaping SAR ADC achieves commendable SNDR and SFDR with reasonable power consumption at 65 nm CMOS technology. By employing error feedback around the SAR-ADC, quantization noise is significantly reduced, resulting in a FoM of 11.99 fJ/step. With an input bandwidth of 625 kHz, this work achieves a sharp Noise-Transfer-Function (NTF). Several other advancements in design of hybrid ADCs are presented in Ref. [21].

Considering the performance of the proposed ADC summarized in Tables 2 and it offers simplicity, lower power consumption, and compatibility with supply voltages as low as 0.7V. It operates over the widest temperature range, from −55 °C to +125 °C, and achieves the lowest DNL/INL values. Due to the large sampling capacitor and the on-chip decoupling capacitors used to purify reference voltages, the occupying area is notably large. Despite its lower measured SNDR compared to Refs. [17,16], it excels in FoM, boasting a low value of 4.5 fJ/step.

5. Conclusion

This paper introduces a 12-bit, 100 kS/s SAR ADC exhibiting remarkable robustness in the presence of mismatch, temperature and process corners. The ADC, due to a large unit capacitor, occupies a relatively large area of 0.6 mm^2, a constraint imposed by the foundry. Thanks to the DAC switching scheme as well as developed circuit

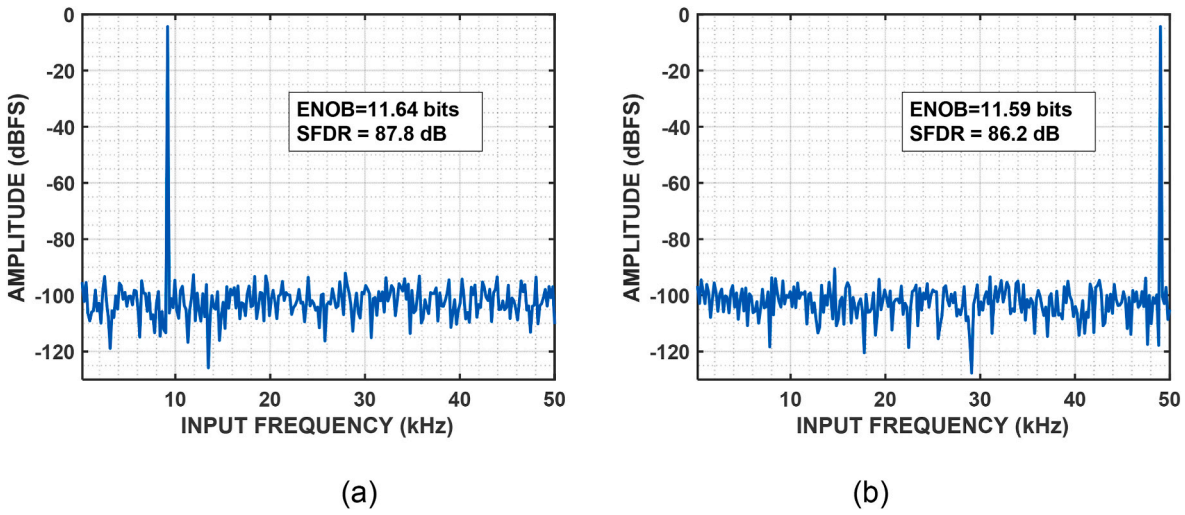

Fig. 14. output fft result of the ADC at $f_S = 100$ kHz, $V_{IN} = -3.8$ dBFS and (a) $f_{IN} = 9.179687$ kHz (b) $f_{IN} = 49.023437$ kHz.

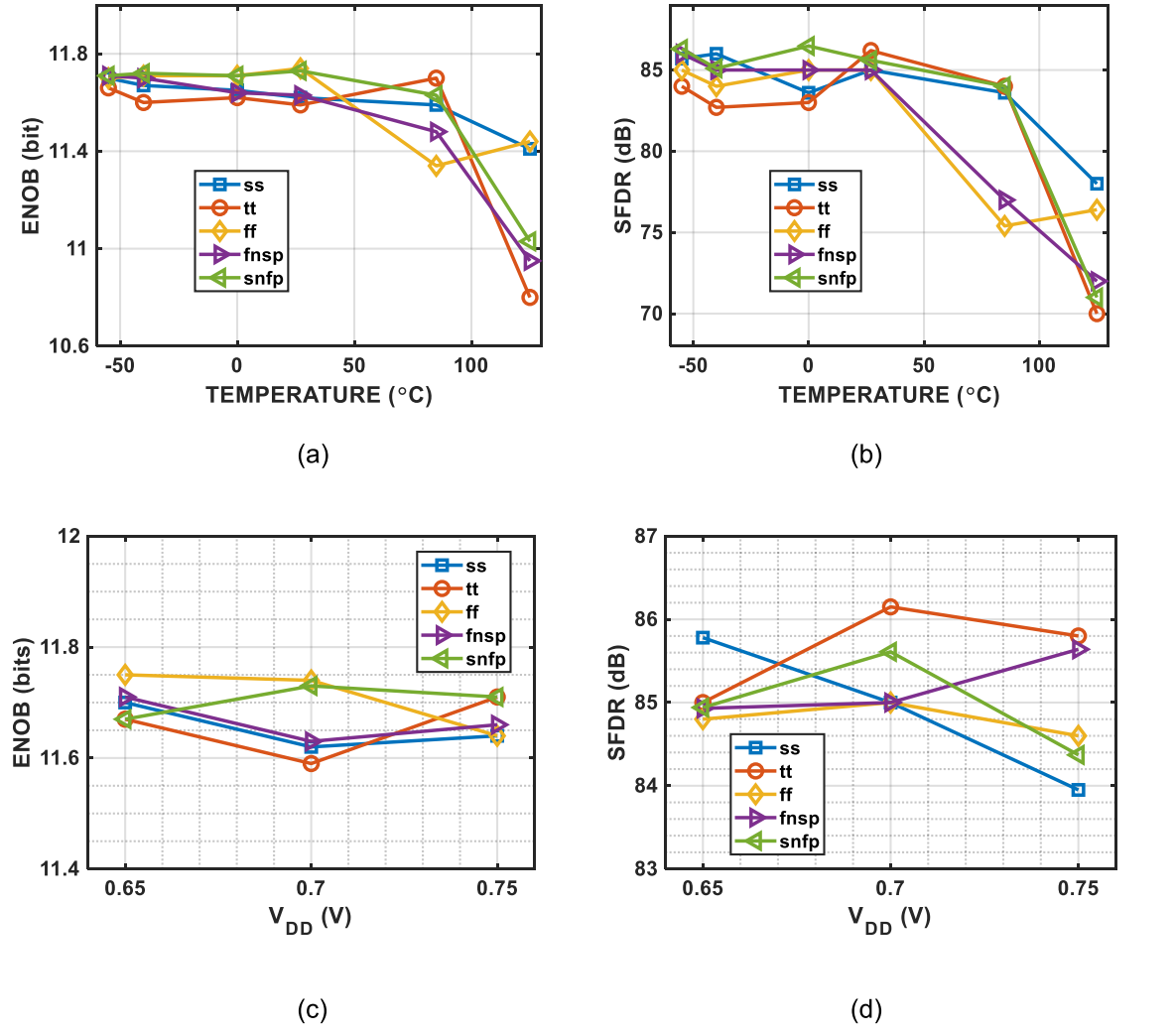

Fig. 15. (a) ENOB and (b) SFDR vs. Temperature with $V_{DD} = 0.7$V. (c) ENOB and (d) SFDR vs. V_{DD} at 27 °C. In all results, the input is at the Nyquist frequency.

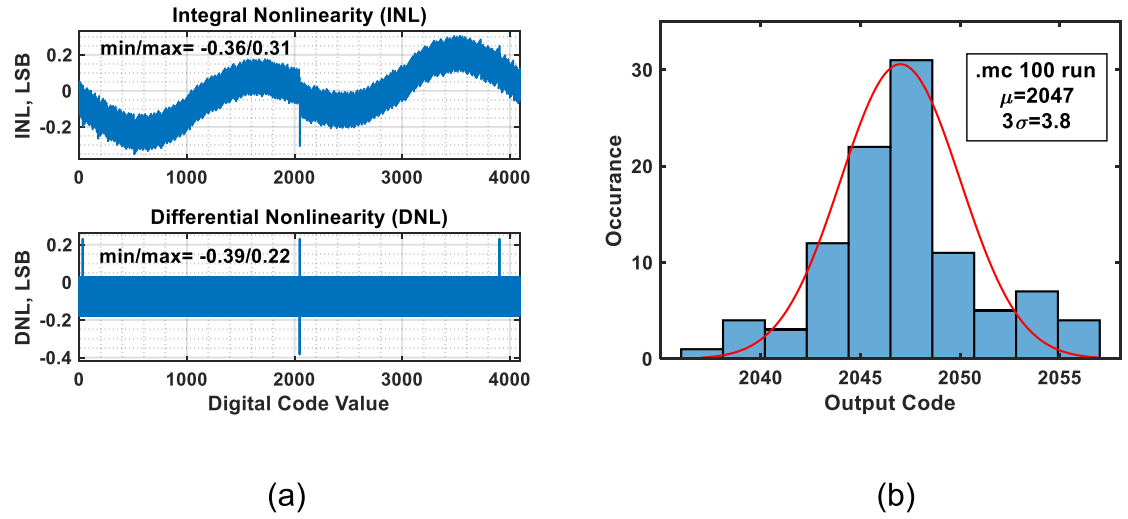

Fig. 16. (a) INL and DNL plots (b) Output code with inputs shorted to V_{CM}.

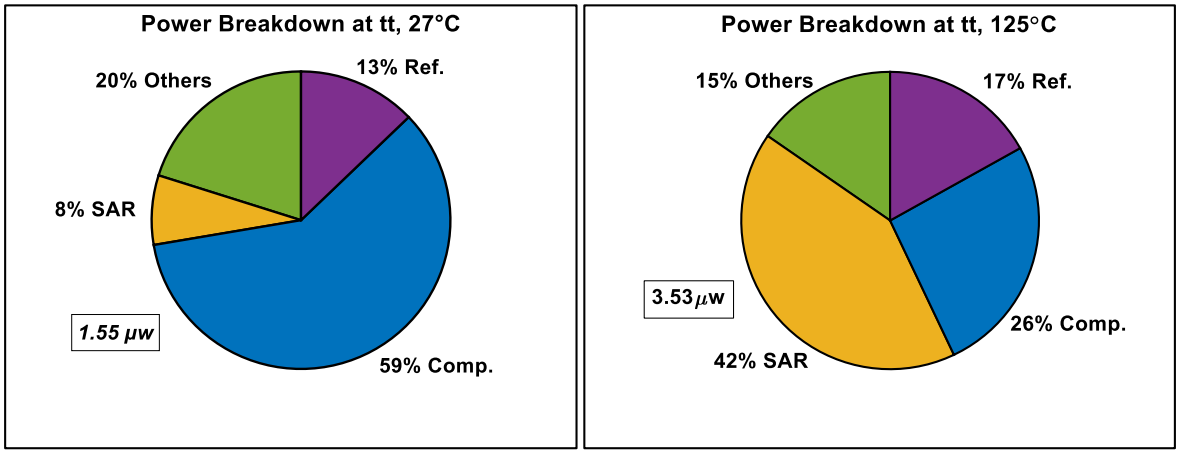

Fig. 17. Power breakdown of the ADC

Table 2
Performance summary.

	This Work 2024	[16] 2022	[1] 2016	[17] 2023	[18] 2020	[19] 2022	[20] 2023
Tech. (nm)	**65**	65	65	180	180	180	180
Sampling Freq. (kHz)	**100**	2 × 625	80	2 × 20	100	200	2 × 25
No. of bits	**12**	–	10	12–18	12	12	–
Sampling Cap. (pF)	**13.3**	2.4	0.256	12	0.95	–	–
V_{DD} (V)	**0.7**	1.2	0.8	1.8	0.7	1.8/1	1
SNDR (dB)	**72.4**	79.3	56.6	71.6–102.8	63.7	67.4	64.5
SFDR (dB)	**86**	90.4	65	75–105	84	73.5	–
DNL/INL (LSB)	**−0.39, + 0.22/-0.36, + 0.31**	–	0.94/0.6	–	±0.45/−0.55, +0.65	–	–
Power diss. (μw)	**1.55**	113.02	0.106	520–1300	1.15	5.05	506
Temp.	**−55°C – + 125°C**	–	–	–	–	–	–
Area (mm^2)	**0.6**	0.354	0.26	1.01	0.06	0.7	0.248
FoM (fJ/step)	**4.5**	11.99	2.4	4180–287	6.6	13.2	7370
Calibration	**No**	No	No	No	Yes	Yes	No

techniques, the proposed SAR ADC stands out in performance. It achieves a power consumption of only 1.55 μW from a 0.7V supply voltage, showcasing resilience to temperature variations ranging from −55 °C to +125 °C and ≃±10 % variations in the supply voltage V_{DD}. The Figure-of-Merit of the proposed ADC is measured at 4.5fJ/step.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

References

[1] M. Liu, et al., A106nW 10 b 80 kS/s SAR ADC with duty-cycled reference generation in 65 nm CMOS, IEEE J. Solid State Circ. 51 (10) (2016) 2435–2445.
[2] Z. Zhu, Y. Liang, A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18um CMOS for Medical Implant Devices, IEEE Transactions on Circuits and Systems I: Regular Papers 62 (9) (Sept. 2015) 2167–2176.
[3] C.C. Liu, et al., A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure, IEEE J. Solid State Circ. 45 (4) (2010) 731–740.
[4] P. Harpe, et al., A 0.20 mm2 3nW signal acquisition IC for miniature sensor nodes in 65 nm CMOS, IEEE J. Solid State Circ. 51 (1) (Jan. 2016) 240–248.
[5] Y. Liang, et al., SAR ADC architecture with 98.8 % reduction in switching energy over conventional scheme, Analog Integr. Circuits Signal Process. 84 (2015) 89–96.
[6] T. Yousefi, A. Dabbaghian, M. Yavari, An energy-efficient DAC switching method for SAR ADCs, IEEE TCAS II: Express Briefs 65 (1) (Jan. 2018) 41–45.
[7] C. Yuan, Y. Lam, Low-energy and area-efficient tri-level switching scheme for SAR ADC, Electron. Lett. 48 (9) (Apr. 2012).
[8] Y. Hu, A. Liu, B. Li, Z. Wu, Closed-loop charge recycling switching scheme for SAR ADC, Electron. Lett. 53 (2) (2017) 66–68.
[9] I. Ndip, et al., Modeling and minimizing the inductance of bond wire interconnects. 17th IEEE Workshop on Signal and Power Integrity, 2013, pp. 1–4. Paris, France, 2013.
[10] Behzad Razavi, Design of Analog CMOS Integrated Circuits, 587.589, McGraw-Hill, New York, NY, 2001, pp. 83–90, 2017.
[11] Behzad Razavi, The bootstrapped switch [a circuit for all seasons], IEEE Solid-State Circuits Magazine 7 (3) (2015) 12–15.
[12] S. Narendra, et al., Scaling of stack effect and its application for leakage reduction. ISLPED'01: Proceedings of the 2001 International Symposium on Low Power Electronics and Design, 2001, pp. 195–200. Huntington Beach, CA, USA.
[13] H. Xu, A.A. Abidi, "Analysis and Design of Regenerative Comparators for Low Offset and Noise," in, IEEE Trans. Circ. Syst. I: Regul. Pap. 66 (8) (Aug. 2019) 2817–2830.
[14] Chengcheng Zhang, et al., " A 0.4-to-0.8 V 0.1-to-5 MS/s 10 b two-step SAR ADC with TDC-based fine quantizer in 40-nm CMOS", Microelectron. J. 141 (2023) 105974.
[15] Y. Liang, C. Li, S. Liu, Z. Zhu, A 14-b 20-MS/s 78.8 dB-SNDR energy-efficient SAR ADC with background mismatch calibration and noise-reduction techniques for portable medical ultrasound systems, IEEE Transactions on Biomedical Circuits and Systems 16 (2) (April 2022) 200–210.
[16] P. Yi, et al., A 625kHz-BW, 79.3dB-SNDR second-order noise-shaping SAR ADC using high-efficiency error-feedback structure, IEEE Transactions on Circuits and Systems II: Express Briefs 69 (3) (March 2022) 859–863.
[17] Y. Liang, et al., A reconfigurable 12-to-18-Bit dynamic zoom ADC with Pole-optimized technique, IEEE Transactions on Circuits and Systems I: Regular Papers 70 (5) (May 2023) 1940–1948.
[18] Y.-H. Chung, Q.-F. Zeng, A 12-bit 100-kS/s SAR ADC for IoT applications. International Symposium on VLSI Design, Automation and Test, 2020, pp. 1–4.
[19] Nguyen, et al., A 12-b sub-ranging SAR ADC using detect-and-skip switching and mismatch calibration for biopotential sensing applications, Sensors 22 (2022) 3600.
[20] Z. Yu, et al., A time-domain reconfigurable second-order noise shaping ADC with single fan-out gated delay cells, IEEE Trans. Very Large Scale Integr. Syst. 31 (6) (June 2023) 902–905.
[21] Y. Zhang, Z. Zhu, Recent advances and trends in voltage-time domain hybrid ADCs, IEEE Transactions on Circuits and Systems II: Express Briefs 69 (6) (June 2022) 2575–2580.